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NAVAL AIR WARFARE CENTER WEAPONS DIVISION
CHINA LAKE, CA 93555-6001

Naval Air Warfare Center Weapons Division

FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Air Warfare Center Weapons Division (NAWCWPNS), as supporting documentation for the 18th Annual Electronics Manufacturing Seminar to be held 23–24 February 1994 and sponsored by NAWCWPNS, China Lake, Calif. This document is a compilation of information that was provided by both nongovernment and government sources.

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Approved by
A. K. ROGERS, *Head*
Engineering Department

Under authority of
D. B. McKINNEY
RAdm., U.S. Navy
Commander

Released for publication by
S. HAALAND
Deputy Commander for Research and Development

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13. ABSTRACT *(Maximum 200 words)*

(U) Presented are the proceedings of the 18th Annual Electronics Manufacturing Seminar, held on 23–24 February 1994, in Ridgecrest, Calif. The proceedings include the papers presented at the Seminar and cover all aspects of soldering technology and electronics manufacturing. The proceedings are a compilation of information provided by both nongovernment and government sources. The proceedings are published in the interest of furthering communication and broadening awareness of current activities among soldering technology and electronics manufacturing specialists.

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Finite element modeling
No-clean soldering process
Lead-free solders
Wetting balance
No-clean fluxes
Wave soldering process improvement
Surface-mount solder reliability
Solder paste in ultra fine pitch era
Certification and training trends

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INTRODUCTION

The continued success of the electronics manufacturing segment of the U.S. defense industry depends heavily upon ever-increasing cooperative efforts between government, industry, and academia. Shrinking defense budgets mandate that every defense dollar be invested wisely to prevent erosion of our superb defense capabilities. The 18th Annual Electronics Manufacturing Seminar affords the opportunity for defense industry partners to exchange ideas, review emerging technologies, and establish relationships to foster continually increasing cooperative efforts. The synergy resulting from increased cooperation within the defense industry partnership will enable the U.S. to effectively meet the defense challenges of the 21st century.

Environmentally responsible design and manufacturing continue to be extremely important aspects of our industry. However, we must not lose sight of the fact that the application of research developments and advanced technology are crucial to the development of advanced weapon systems. Thus, our challenge is to develop advanced weapon systems within the constraints imposed by declining budgets and environmental pressures.

Productivity, producibility, and quality continue to be the goals we must all pursue. By focusing on these goals, each of us will be doing our part to ensure that affordable, reliable weapons are available for our troops. Through effective improvement and expansion of the use of the best practices available within the U.S. electronics industrial base, collectively we will be able to meet these goals. The Product Assurance Branch of the Naval Air Warfare Center Weapons Division at China Lake is committed to supporting continual improvement of electronics manufacturing capabilities within the U.S.

We look forward to working with you to improve our electronics manufacturing industrial base. We appreciate your interest in electronics manufacturing and thank you for joining us at the 18th Annual Electronics Manufacturing Seminar.

Ray Terry, Head
Product Assurance Branch
Product Support Division
Engineering and Logistics Department

TESTING OF ALTERNATE CLEANING MATERIALS AND ALTERNATE FLUXES FOR REWORK AND REPAIR

by

John Fischer, Jim Smith, Jerry Maurice, Roger Nickell,
Loretta Lusk, Robin Nissan, Larry Merwin, and Greg Ostrom
Naval Air Warfare Center Weapons Division
China Lake, CA 93555

Because of the high interest in a new water soluble flux known as HF1189 (invented and patented by Hughes), we decided to concentrate the initial portion of our program to investigating this material. Preliminary results of this effort were reported at the China Lake 18th Annual Electronics Manufacturing Seminar. The goal of this particular task was to determine if this flux would be suitable for Navy use in rework, repair, and maintenance of electronic hardware as well as the initial manufacture. Chemically, HF1189 is simply citric acid (derived from citrus fruit) in water. Citric acid is highly soluble in water which allows simple water washing of hardware after soldering totally eliminating the need for ODC solvents. HF1189 is non-toxic, contains no VOC's, and does not involve expensive disposal procedures. Since the military has not allowed the use of water soluble flux in the past because of potential corrosion problems, our program has been aimed at determining the long term effects of using this new material.

The test printed circuit assembly (PCA) used for evaluation has been a non-functional double sided printed wiring board (PWB) containing exclusively plated through hole components. This assembly is the standard used in the Department of Defense (DoD) soldering certification centers within the Navy and the Army. Fabricated from FR-4 epoxy glass material, the PCA contains 15 resistors, 10 capacitors, 8 diodes, 3 dual in line packages (DIP's), 7 transistors, and a large tin-lead plated ground plane. This assembly measures 3 by 4 inches. We chose this assembly because it is inexpensive, readily available, soldering parameters are well known, and is representative of the type of material and configuration found in many Navy electronic packages. Performance was measured against currently used rosin (RMA) flux.

Both wave soldering and hand soldering were easily accomplished using HF1189. Wave soldering produced less defects than RMA flux. Hand soldering using HF1189 cored 63/37 tin-lead solder required the operator to modify techniques as compared to RMA flux. This was a small obstacle which has been readily overcome with practice. No new soldering equipment was required to transition from RMA to HF1189 with the exception of a new fluxing stone on a wave soldering machine. This was required to ensure no rosin flux residues would contaminate a PCA.

Because the program did not allow the purchase of new capital equipment, we built two batch type aqueous cleaners. These cleaners use 18 megohm deionized water which is heated to approximately 140 - 160° C as per the recommendation from Hughes. The apparatus were constructed from inexpensive commercially available pumps, nozzles, etc., such that the design could be transitioned to a NADEP or other activity which may not be able to purchase new equipment in a timely manner. The details of the design are available to any interested person.

Aqueous cleaning of citric acid residues after hand or wave soldering was an efficient process as would be expected because of the high solubility of citric acid in water. PCA's soldered with either wave or hand techniques presented no cleaning problems if they were cleaned within one-half hour of the soldering operation. Because of mil-spec requirements, we cleaned our assemblies within one hour to simulate actual assembly conditions. All tested PCA's passed Mil-Std-2000 ionic cleanliness requirements of maximum 10 micrograms per square inch of sodium chloride equivalents. Ionic cleanliness measurements were recorded on an Omegameter at ambient temperature using a 75% isopropyl alcohol 25% water solution.

Because ionic cleanliness may not be an accurate test to measure residues on a PCA, ion chromatography offers an alternative analysis technique. The method employed for citrate ion analysis was conducted on a Dionex 4500i instrument with AS-5 columns and an anion/organic acid analysis method. PCA's after soldering and cleaning were extracted with deionized water; the aqueous extracts were then analyzed for citric acid and measured against a known standard. Table 1 provides a list of results from ambient and boiling water extraction of several PCA's after cleaning with our batch aqueous cleaning system.

TABLE 1. Results of PCA water extract citric acid analysis.

PCA #	WATER TEMP (^{o}C)	DWELL TIME	CITRIC ACID ($\mu g/in^2$)
1	100	15 min	6
2	100	15 min	7
12	100	15 min	9
16	100	15 min	11
17	100	15 min	6
18	100	15 min	13
23	100	15 min	18
24	100	15 min	14
25	100	15 min	10
14	20	24 hrs	6
21	20	24 hrs	6
16	20	24 hrs	6
2	20	24 hrs	6
20	20	24 hrs	6
23	20	24 hrs	6
5	20	48 hrs	6
15	20	48 hrs	6
13	20	48 hrs	7
25	20	48 hrs	7
21	20	48 hrs	6
12	20	48 hrs	6
17	20	120 hrs	6
18	20	120 hrs	6
19	20	120 hrs	6
20	20	120 hrs	6
24	20	120 hrs	6
1	20	120 hrs	6

Note: PCA's 1, 2, 12, 16, 17, 18, 23, 24, and 25 were initially extracted with ambient temperature water followed by boiling water Total amount of citric acid residues on these assemblies are determined by addition of the two citric acid residue analysis results.

Currently, no military specification exists for maximum allowable limits of citric acid residues. Because PCA's cleaned in an identical manner passed ionic cleanliness testing, it appears that slightly elevated citric acid residues are not a problem. The mil-spec ionic cleanliness test was designed to measure residual alkyl amine hydrogen halides (bromide or chloride) which have been added as activators to RMA flux. These compounds release hydrochloric or hydrobromic acid upon exposure to a moist or humid environment which initiates dendritic growth and corrosion between active circuit traces on PCA's. The conductivity of these materials is important. As a comparison, table 2 lists conductivity values of hydrogen bromide, hydrogen chloride, and citric acid as a function of concentration in water at 18°C.

Table 2. Electrical conductivity of HCl, HBr, and citric acid in water at 18°C (source - Lange's Handbook of Chemistry, 12th ed.).

ACID	CONCENTRATION (N)	CONDUCTIVITY (ohm^{-1}-cm^2-$equiv^{-1}$)
HBr	0.1	356
HCl	0.1	351
citric	0.1	16.1

Because citric acid is a poor conductor relative to the conventional flux activators, it is unlikely that slightly elevated citric acid residues will present a problem with dendritic growth.

As a comparison, we assembled and cleaned several PCA's at Texas Instruments in Lewisville, TX. This facility has a large production capable in-line aqueous cleaner which is used on a number of military programs. Four PCA's were extracted with boiling deionized water for 15 minutes each and the water extracts analyzed for citric acid by the above method. Three of the boards had levels of 0.2 and the fourth had 0.3 micrograms per square inch of citric acid residues. This result suggests that an efficient commercially available cleaning system can remove any significant traces of citric acid.

Analysis of thermal degradation products of citric acid was done to determine if citric acid degraded to more or less active chemical species. Samples of neat citric acid were heated in liquidus solder for varying lengths of time (5 seconds to 1 minute) and the thermolysis products were analyzed using nuclear magnetic resonance (^1H and ^{13}C NMR), gas chromatography-mass spectroscopy (GC-MS), and Fourier transform Infra-red spectroscopy (FTIR). Products have been identified as citriconic acid, citriconic anhydride, itaconic acid, and itaconic anhydride. All of these compounds are less acidic and chemically active than citric acid.

Long term reliability has always been an important issue with military hardware. To address this topic, twelve PCA's were artificially aged. To simulate a worse case scenario, the assemblies were hand soldered using an excessive amount of HF1189 to

ensure that the most active chemical species would be present on the PCA's. PCA's #80 and 81 were soldered, cleaned with our in-house batch cleaner, and conformally coated with polyurethane. PCA's #82 and 83 were soldered, brushed with excessive HF1189, and cleaned with our in-house batch cleaner. PCA's #87 and 88 were soldered and not cleaned. PCA's #89 and 90 were soldered and cleaned with cold tap water, 30 seconds per board side. PCA's #91 and 92 were soldered with RMA flux and cleaned with trichloroethane in a vapor degreaser (benchmark). PCA's #93 and 94 were soldered, cleaned with our in-house batch cleaner, and not conformally coated. In addition, 30 gold cup wire assemblies were fabricated as per Mil-Std-2000 requirements with the exception that the wire (stranded, nickel plated) was not tinned prior to soldering. Ten of the wires were cleaned with deionized water, ten wires were cleaned with isopropyl alcohol, and ten wires were left uncleaned. All of the assemblies were placed in a temperature-humidity chamber at 70°C and 85% relative humidity for 21 days. This condition simulates a storage or 15 years at 30°C and 50% relative humidity. The results are shown in table 3.

Table 3. Results of accelerated aging test.

PCA #	OBSERVATIONS/RESULTS
80 & 81	no indication of corrosion, conformal coating uniform, no delamination of conformal coating, high luster of base metal
82 & 83	no indication of corrosion, all components and board laminate appear intact, no materials compatibility problems seen
87 & 88	heavy corrosion of soldered surfaces, heavy corrosion of component leads, component bodies and board material intact
89 & 90	no visible corrosion, small traces of white residues under components, no effect on base metal
91 & 92	no corrosion, high luster of base metal
93 & 94	no corrosion, high luster of metal on components, low luster of soldered surfaces, no base metal degradation
water cleaned wires	no corrosion on exposed wire or under insulation
IPA cleaned wires	no corrosion on exposed wire or under insulation
uncleaned wires	corrosion on exposed wire surfaces

All of the wires were pull tested to failure. In all cup assemblies, the solder joint remained intact. Failure was due to wire breakage well above the solder joint. This results suggests that use of HF1189 does not require pre-tinning in cup assemblies and simple warm deionzed water washing will remove corrosive materials. This test will be

repeated to verify the findings. A detailed analysis to study the effects of HF1189 on stranded wire is planned for fiscal year 1994.

In one instance, a PCA was not cleaned within one hour of soldering. Time interval between soldering and cleaning was estimated to be 6 hours. After cleaning of this assembly, a "white" residue was observed on the ground plane. FTIR analysis revealed that no organic compound was present. Scanning electron microscopy (SEM) showed that this residue was a small surface pit in the tin-lead plate. No base metal was exposed to adversely effect long term reliability.

An FTIR instrument equipped with an IR microscope was used to detect the presence of citric acid residues in likely areas of entrapment, i. e., under component bodies, between leads, etc., on cleaned assemblies. No evidence of citric acid or other organic residues was found.

Thermal shock of several assemblies which were soldered and cleaned show no negative effects as compared to assemblies soldered with RMA flux and cleaned with trichloroethane in a vapor degreaser. The conditions of the test were as per Mil-Std-202 test condition A2. The PCA's were taken from ambient and quickly placed in a freezer at -55^{o}C for 5 minutes, quickly removed and held at ambient for 5 minutes, then quickly placed in an oven at +85^{o}C for 5 minutes. This cycle was repeated 50 times. The solder exhibited the typical grain formation and loss of metallic luster which was expected of tin-lead solder. No cracked or failed solder joints have been observed.

A proposed mechanism of action of citric acid to explain high efficiency as a soldering flux is chelation of metal oxides. Questions have been raised as to the fate of these chelates if indeed they do form at an appreciable level. Using NMR techniques, citric acid chelates (salts) of copper, tin, and lead have been made and characterized. To date, no chelates have been found on any of the PCA's in our study.

Three new water soluble fluxes manufactured by Alpha Metals were also investigated . These materials have been qualified to MIL-F-14256F category WSF-O. This designation is for water soluble fluxes which are polyglycol free. The Alpha brand names are WS-651 (contains halides), WS-360, and WS-630 (360 & 630 are halide free). Each flux was chemically analyzed and found to consist of a mixture of water soluble organic acids in addition to low levels of wetting agents in isopropyl alcohol. Several printed circuit assemblies (PCA) were soldered with each of these new fluxes and cleaned with the simple deionized water system described above. Temperature of the wash water was maintained at 160^{o}F. All of the PCA's passed ionic cleanliness measurements as per MIL-STD-2000 (all ionic contamination was well below 10 micrograms / square inch of board surface).

Quality of solder joints was good; solder joint defect levels were low. The majority of the PCA's exhibited a dull appearance on the surface of the solder. This effect was reduced if the PCA's were first rinsed with a slightly basic (pH=8) water wash then cleaned with warm deionized water. After several discussions with electronics manufacturers, we believe that this dull luster is of no concern. We have attempted to identify the material causing this appearance as have a number of military electronics

manufacturers. No conclusive identification has yet been achieved. We do not believe this cosmetic characteristic is a problem for long term reliability.

A long term aging test was done as previously described. Nothing unusual was seen from this test. PCA's coated with a polyurethane conformal coating showed good adhesion of the coating. No corrosion was identified on any of the cleaned PCA's. As expected however, uncleaned assemblies did exhibit severe corrosion. This demonstrates the importance of cleaning these flux residues from the PCA's.

A series of stranded wires (nickel plated, teflon insulation) were soldered into gold cup terminals. Test sets included wires which were pretinned, not pretinned, no post soldering cleaning, post soldering cleaning with water or isopropyl alcohol. All of the wires were aged as above. The majority of the wires exhibited either mild corrosion under the wire insulation or the presence of a white solid. Analysis of the solid suggests that the chemical composition is either an inorganic carbonate or a mixture of organic acids. Alpha Metals does not recommend use of these fluxes for the tinning or soldering of stranded wire.

A set of the PCA's after cleaning were further extracted with boiling deionized water and analyzed by ion chromatography. As expected, low levels of the flux organic acids were found. The levels were very low and are comparable with the amounts of HF1189 residues. No appreciable amounts of ionic contamination were found.

Detailed surface analysis of the PCA's by Fourier Transform Infrared Spectroscopy (FTIR) did not detect any significant amounts of organic residues. Chemical degradation products of the flux constituents are known. Our analysis did not detect any of these materials.

China Lake also investigated new organic cleaning solvents for bench top cleaning after rework and repair with RMA flux. Our testing included visual inspection, ionic cleanliness (as per MIL-STD-2000), HPLC analysis of residues (organic acids from flux), FTIR surface analysis, materials compatibility, and chemical analysis of cleaning agents. Materials compatibility testing exposed a series of commonly used electronics PCA materials to the solvent for 1, 24, and 48 hours. We examined the specimens for swelling, desorption of the solvent, and material degradation. The materials studied were: FR4 epoxy glass and polyimide printed wiring board laminates, polyethylene (shrink tubing), nylon 66 (harness tie wrap), epoxy bodied components, teflon, kalrez (fluoroelastomer), viton SZ (fluoroelastomer), PTFE/propylene copolymer, EP epoxy, silicone rubber, and standard marking inks. The elastomers studied would be in gaskets and seals of components and assemblies. This list is only representative of common materials. Users are cautioned to conduct simple exposure tests if there are any compatibility concerns. We did not extensively test conformal coatings. Because of the wide variety of coatings and new solvents, we recommend that all conformal coating be removed before any new solvent is used unless specific data exists to support compatibility.

Because of the wide variety of available solvents, our goal is not to develop an approved list. We intend to gather data of different solvent types and formulations which will be used to develop specifications for Navy maintenance manuals.

A major program beginning early 1994 is a joint effort between China Lake, the Georgia Institute of Technology, NASA, Army MICOM, Rome Air Development Center, and several DoD electronics manufacturers. This task will investigate several basic questions and issues regarding alternative materials and processes to currently used ozone depleting chemicals (ODC) used in the fabrication of military electronics. Following is a brief description of the program. Scheduled completion date is 1995.

The ODC alternative technologies being investigated include:

1. Semi-aqueous cleaning of RMA flux. Emphasis of this work is on use of centrifugal cleaning equipment employing terpenes in surface mount technology applications.

2. Semi-aqueous cleaning of RMA and RA flux using in line and batch cleaning equipment.

3. Removal of RMA flux residues with aqueous detergent and saponifiers.

4. Machine soldering with water soluble fluxes and subsequent aqueous cleaning.

5. Controlled atmosphere wave soldering using adipic/formic acid as flux.

Test vehicles are being prepared to evaluate a wide array of applications and process parameters which represent a variety high reliability electronics. The test vehicles will be used to assess long term reliability of alternative manufacturing processes and materials which will satisfy users of high reliability electronic hardware. There are two long-term tests which will be performed as part of this program, namely (1) surface insulation resistance (SIR) testing which provides indications of the effects of alternate materials on the printed wiring board (PWB) substrates, and (2) environmental stress screening (ESS) where the assembled hardware is stressed to failure to determine the failure modes. SIR is evaluated using an interdigitated comb pattern which is placed under a bias voltage in an environmental chamber (usually 85^{o}C/85%RH) with periodic measurements of the insulation resistance between the track. These values are assessed in relationship to unprocessed control coupons. ESS uses an assembly and provides several different stresses (temperature cycling, humidity, vibration, etc.) simultaneously or in series to probe the failure modes.

All new technology developed and evaluated under this program must meet the end item requirements of high reliability electronics specifications such as Mil-Std-2000 to gain acceptance by the military community. Currently established benchmarks of RMA flux followed by cleaning with ODC's serve as the baseline. Alternative technology which falls below this baseline is not accepted for use in a high reliability scenario. SIR and ionic cleanliness requirements must meet the parameters established in Mil-Std-2000 as a minimum. Because technology is being investigated which has little or no performance history, it is important to prove long term performance. To this end, extensive ESS evaluation will be performed. Guidance for this analysis is found in Mil-

Std-202 (test methods for electronic and electrical component parts) and Mil-Std-883 (test methods and procedures for microelectronics). Both of these documents are referenced in Mil-Std-2000. The ESS program essentially subjects electronic assemblies manufactured with alternate processes to simulated severe environmental conditions. These conditions consist of extremes in temperature, humidity, and long term storage. Data gathered from this analysis will predict long term reliability and performance of the hardware. New processes or materials examined in this program which induce failures earlier than the current benchmark will not be recommended for adoption to the high reliability electronics manufacturing community.

As part of the ESS evaluation, an accelerated aging analysis of production hardware manufactured with alternate methods must be done. Hardware which is functional and well characterized will be used for evaluation. Acceptance criteria is if the performance is within the defined parameters after 20 years of simulated aging. When possible, assemblies will be tested to failure. A complete failure analysis will be done to determine what expected life times and reliability will be as a result of new processes.

An integral part of the ESS testing is a detailed analysis of the degradation which was induced in the solder joints and in the PWB's. A statistically significant number of solder joints will be micro sectioned and thoroughly analyzed using metallographic techniques. We will determine if new fluxes, cleaning techniques, or soldering methods induced degradation beyond what normally occurs with current processes. Also, mechanical pull testing to determine solder joint strength will be done to ensure that joint strength has not been compromised. The PWB materials, e.g., FR-4 epoxy glass, polyimide, etc., will be examined after processing with the new technologies to examine material compatibilities. All new accepted processes and materials must be compatible with the PWB materials employed by the users and manufacturers of high reliability electronics.

In addition to examining the reliability and performance of electronic assemblies fabricated with new materials and processes, the effect of these processes on discrete components will be examined. The main concern here is corrosion. Issues addressed include: (1) the reliability of non-hermetically sealed components after water washing, (2) the long term effects of using alternate fluxes on the cases and lead seals of components, and (3) the possibility of corrosion or degradation of metal and polymeric component cases. A circuit assembly chosen for evaluation must be representative of both present and future technology which results in a mixture of packaging technologies. Components from ESS tests will be evaluated by a number of techniques including: optical inspection, scanning electron microscope, energy dispersive x-ray analysis, x-ray inspection, surface chemistry and material characterizations.

A flux corrosion test is being developed for the purposes of screening soldering fluxes for their "corrosion potential". This test evaluates the ability of flux residues to corrode a thin copper track. Recent developments at Georgia Tech have lead to a modified test coupon which appears to be very sensitive to corrosion measurements. The test method has been developed using poorly cleaned water soluble flux residues. Extensive work is now underway with a variety of fluxes to establish a measure of (1) low corrosivity, (2) moderate corrosivity, and (3) high corrosivity. This test can also

benchmark the presently used rosin flux/cleaning process and compare the results to the alternative cleaning systems under investigation. This test can also be used to assess the corrosivity of low solids/no clean fluxes, residues from controlled atmosphere wave or reflow soldering processes, and water cleaned/water soluble flux residues.

Research is also underway to examine the relationship between SIR readings and electrochemical migration. Some recent industry tests of flux alternatives have been performed in a condensing environment and have shown electrochemical migration. This failure mechanism is not observed when the test is run in a non-condensing environment. Clarification is needed on the proper way to conduct SIR tests and the variation in meaning between the test results associated with humidity acceleration and that associated with a condensing environment. There are indications in the literature that the water drop test accelerates failure mechanism on ceramic devices that are not found in normal operating conditions. In addition, the accelerating factor is 10^4 times as fast in the condensing environment than in the high humidity environment. A clearer understanding of the significance of SIR data as it relates to water soluble fluxes and low solids fluxes needs to be obtained since this test is widely accepted as a qualification standard for high reliability electronics applications.

While the flux residue corrosion test mentioned above deals with the degradation of the metal conductor, SIR testing has historically been used to measure the electrical characteristics of the substrate, i. e., its resistance to current leakage. As these substrates are processed with new materials such as the cleaning alternatives and flux alternatives defined in this study, the SIR test has been used to assess and predict field failures. Unfortunately, the present tests were developed with rosin flux chemistry and new materials may require different assessment conditions. The increase in circuit density of today's assemblies leads to the question of the proper test vehicle and test conditions for SIR evaluation. Variability in line spacing, accelerating voltage, appropriate temperature/humidity stress conditions, and even variability in testing the vehicles in the "unpowered" state need to be considered.

Coupons are tested to failure and analysis of the material degradation products is performed. Corrosion and the identification of failure due to conductive anodic filament (CAF) is carefully studied. Primarily using analytical electron beam instrumentation (SEM, TEM, microprobe, Auger, etc.) corrosion products, degradation products, micro structural changes and residues are examined and catalogued relative to electrical test results. Surface (top 2-4 nm), and near surface (top 1-2 micron) and subsurface (top 1-2 nm) regions are examined using surface analytical techniques (including XPS and FTIR) and analytical electron beam instrumentation in conjunction with appropriate sample preparation. This includes fractured and polished cross sections as well as etched surfaces. Results of these tests are used to identify mechanism of corrosion and to identify unwanted processing products. Experimental work is directed to the correlation of long term reliability under various temperature and humidity stresses with the residues on the PWB from the soldering process.

A principal limitation of SIR is that it provides less information than required to predict the long term performance of a product. What is required is a series of electrical measurements adequate to simulate product behavior over the intended lifetime of the product in its storage and use conditions. Thus, the development of a new test method

to predict product performance is underway. This work is being done in a joint effort between Georgia Tech, Digital Equipment Corporation, and Motorola.

Product performance depends upon electrical interconnect characteristics. Key characteristics are the resistance of a printed wire and the capacitance of the wire relative to ground as a signal is being transmitted from point A to point B. These depend on the relative dielectric constant of the substrate (e.g., FR-4), the dissipation of the dielectric, and the sheet resistance of the metal. Data on the frequency dependence of these parameters can be used by circuit designers to predict electrical performance. We propose to measure both the frequency and the time dependence of these parameters under accelerating conditions. These data will then be used to predict product performance at a future time by inserting the value of these parameters at time "t" into a circuit simulator. The development of this test method utilizes the same test coupon as the corrosion test described above and requires and impedance analyzer to obtain near open type measurements.

The relationship of the test methods described above to contamination of a PWB is critical. To this end, analytical methods to detect and characterize flux residues are being developed and refined. Work at Georgia Tech is addressing the use of an evaporative light scattering detector along with high performance liquid chromatography (HPLC) to identify polyglycols in water soluble fluxes. This work is currently being expanded to identify and quantify glycols, polyglycols, and polyglycol surfactants. Effort in this area is important to our program because of poor results obtained with available analysis methods for these materials.

Additional work needs to be done on low solids/no clean flux residue detection. These flux detection methods will be used in correlating the failure mechanisms from accelerated life tests with the levels of a particular contaminant. Flux residue detection and characterization is extremely important from a reliability viewpoint. Conformally coated, densely populated high reliability products require complete knowledge of flux residue and its removal. The reliability problems associated with leaving flux residues on a PWB must be assessed. Methods are being developed to examine low residue flux residues. These techniques include various extraction methods and solvents, HPLC analysis, and ion chromatography analysis. The goal is to find the best extraction procedure to efficiently remove flux residues without degrading the laminate material.

China Lake is also participating in a national study determining the viability of no-clean or low residue soldering technology for military hardware. This task, lead by Sandia National Laboratory, is a joint effort between the Departments of Defense and Energy and associated electronics manufacturers. The test program is similar to the plan described above. We are scheduled to complete several SIR tests in early 1994 on a variety of no-clean soldering materials and processes. In addition, investigations into the compatibility of no-clean fluxes and conformal coatings as well as chemical behavior of adipic acid in testing scenarios will begin in 1994.

John Fischer heads the Materials Engineering Branch at the Naval Air Warfare Center Weapons Division (NAWCWPNS), China Lake, California. He has had 7 years of experience as a research chemist and 3 years of experience in soldering technology.

Address: Naval Air Warfare Center Weapons Division
Code C2547
China Lake, CA 93555

Batch Semi-Aqueous Emulsion Cleaning

by

Rex Breunsbach
Electronic Controls Design Inc.
Milwaukie, Oregon

Abstract

Recent development and work with water immiscible Semi-Aqueous solvents at 5%-20% concentration have led to a process that offers significant advantages over full strength Semi-Aqueous, saponification and water-soluble processes. This process uses less solvent, is safer, requires no nitrogen inertion for spray-in-air applications, significantly reduces the cost of rinse water treatment, and lowers equipment costs. This paper examines the effect of process parameters surrounding the emulsion cleaning process and reveals a piece of cleaning apparatus that optimizes the advantages that this process offers.

What is Controlled Emulsion cleaning?

Controlled emulsion cleaning is similar to the 100% or full semi-aqueous cleaning system in that it uses a water-immiscible (gravity-separable) solvent wash followed by water rinsing. Controlled emulsion cleaning uses a 5-20% solvent-water mixture instead of washing with 100% or full-strength solvent. Solvents such as Axarel®-32, Envirosolv® KNI-2000 or Petroferm Bioact®-EC7R are ideal for this process.

The beneficial effect of an emulsion rinse following a full semi-aqueous wash is well documented in in-line cleaning system. The solvent concentration in an in-line emulsion rinse is not controlled, but is simply a byproduct of product flow and drag-out from the wash stage. In the emulsion cleaning process, concentration is carefully controlled.

The batch spray cleaning system is particularly suitable for the controlled emulsion process. Another advantage of the batch spray process is that it does not over-emulsify the mixture thus allowing quick separation on removal of spray emulsifying energy.

Major advantages of Controlled Emulsion Cleaning

Total solution....Wash, Rinse, Dry and Waste Treatment

One of the chief benefits of the controlled emulsion process is that it allows washing, rinsing, drying and waste treatment in one small footprint. The operator does not need to transfer product from the wash to the rinse and dryer modules as required by full semi-aqueous batch equipment. Of course higher throughput can be accomplished with a companion dryer. For safety reasons this companion dryer should be suitable for drying flammable solvents.

Safer....requires no nitrogen

The full semi-aqueous process has two potential safety issues, the fire potential due to flash point and the explosion potential due to the organic mist induced by spraying in air. The controlled emulsion process, if operated at low concentrations with water, obviates the mist explosion potential. However, the flash-point fire potential still exists and washing and rinsing should be done at temperatures below the flash point of the solvent.

IMPORTANT NOTE: Consult your semi-aqueous solvent vendor for proper and safe operation temperatures.

Low process costs

In addition to not requiring expensive nitrogen, the emulsion cleaning process wastes considerably less solvent due to dragout. This means you use less semi-aqueous solvent overall.

Lower waste treatment costs

Lower wash solvent concentration means lower rinse solvent concentration. As there is less solvent in the rinse water, less carbon is required to remove it. Carbon use can be as low as 10% that of full semi-aqueous systems.

Lower equipment and labor costs

The "one chamber" construction of the emulsion cleaning system not only lowers equipment costs, but reduces labor. It is no longer necessary to move product from rinse to wash to drying module.

Total savings of up to 70% over Full Semi-Aqueous !

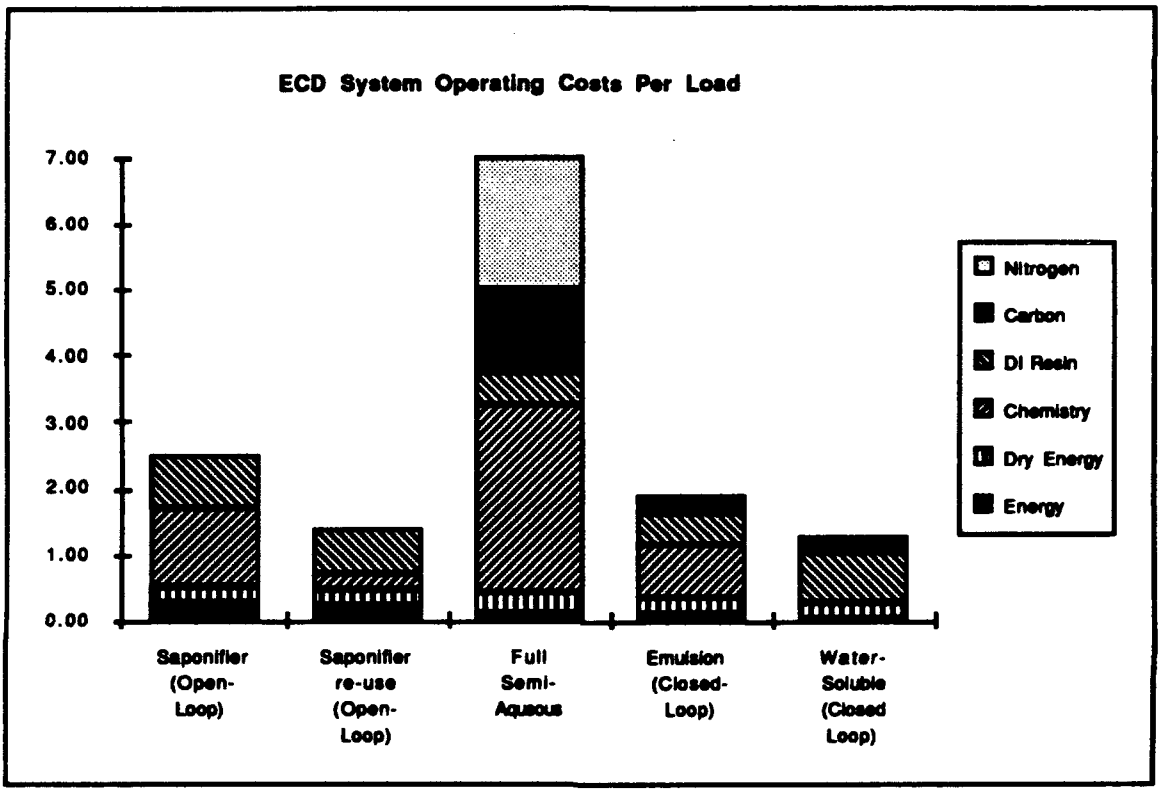

Figure 1.

Total cost savings of the controlled emulsion system are compared to other cleaning alternatives in figure 1. The data in this figure is based on 10 loads per day, 20 square feet per load. The two processes on the left are open-loop saponification. The saponifier re-use process re-uses the wash solution 10 times. The most expensive process is the full semi-aqueous process. This is a 3-module wash,closed-loop rinse and dry. On the right is the water-soluble closed-loop rinsing process. In comparing the full semi-aqueous with the emulsion process, you can see that in addition to the savings in nitrogen costs, carbon and chemistry (solvent) costs are significantly reduced. DI resin use in the saponifier processes is in the treatment of the incoming rinse water. It is interesting that it requires less DI resin to remove the salts from the rinse water in the closed loop processes than to clean up the incoming water in the open loop processes. As you can see, the closed loop controlled emulsion process compares favorably with the open loop saponifier processes.

Advantages compared to other Cleaning Options

Controlled Emulsion Advantages Compared to Full Semi-Aqueous

One of the chief advantages of emulsion cleaning compared to full semi-aqueous is the fact that a complete system can be built with one spray chamber. In the full semi-aqueous system, the wash and rinse stages required two separate chambers, as dragout losses from the wash stage to the rinse were too costly. Another advantage with 5-20% emulsion is the reduction in flammability potential, to the point that nitrogen purging during washing is not required. Of course with lower wash solvent concentrations, the amount of waste solvent in the rinse is greatly reduced, thus reducing treatment costs. Lastly, the "one-chamber" cleaning system can be produced at lower cost than the separate wash and rinsing systems.

Controlled Emulsion Advantages Compared to Saponifier

One of the chief advantages of emulsion cleaning vs. saponifier cleaning is that the organic solvent does not "dull" solder joints like some alkaline saponifier formulations. Another significant advantage is that if rosin removal is not complete, the boards can be re-cleaned. With Saponifiers, if the process is not complete, re-washing is almost impossible due to hydration of the rosin residues. Alkalaline Saponifiers can be difficult to rinse, especially at lower temperatures. If Saponifiers are not adequately rinsed, harmful and corrosive residues can be left on boards..

From a waste treatment standpoint, the emulsion rinse solution is much easier to treat. With gravity-separation (decanting) and carbon adsorption, rinse waste can be economically and simply treated. On the contrary, organic Saponifiers are highly polar and are difficult to remove from the rinse water stream

From an air pollution standpoint, the typical solvent has a lower vapor pressure than most Saponifiers, thus lowering VOC emission levels.

Controlled Emulsion Advantages Compared to Water Soluble Flux

Possibly the most significant advantage of the controlled emulsion cleaning process is that it works with rosin flux and does not require the user to change his process.

Water soluble flux residues can be corrosive and cause equipment failures if not properly removed during cleaning. Semi-aqueous solvent residues are

mostly volatile and evaporate from assemblies.

From a waste treatment point, rosin flux followed by a semi-aqueous cleaning process results in lower rinse water heavy metals content. This lower metals content reduces DI resin requirements in closed-loop rinsing and increases life.

Another advantage of the controlled semi-aqueous process is that organic soils such as finger prints and oils are removed during the rinse process.

What testing says

Phase II Testing

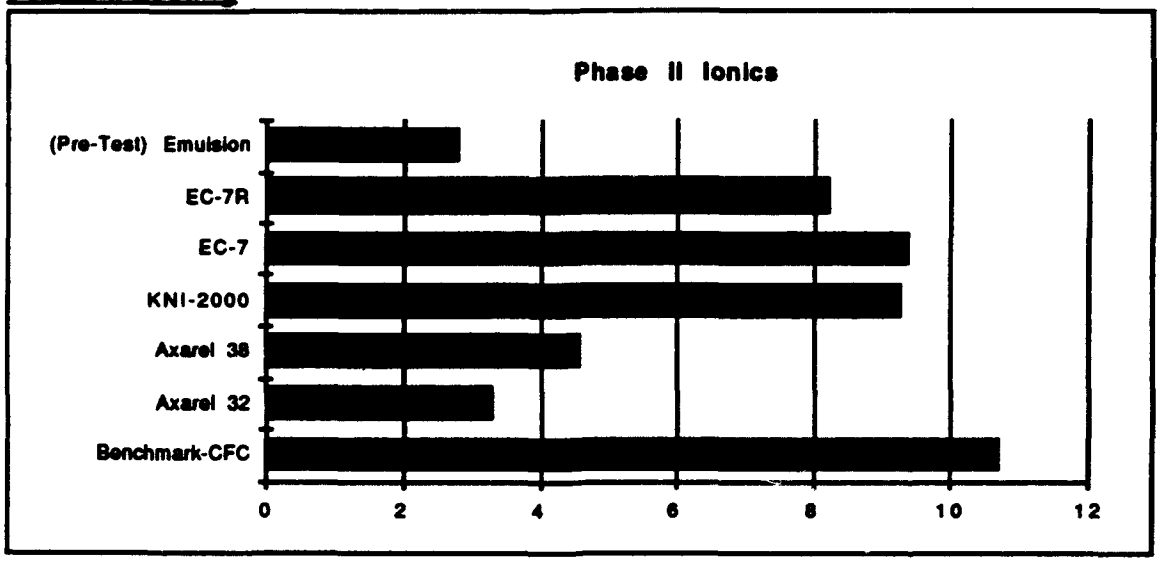

Figure 2.

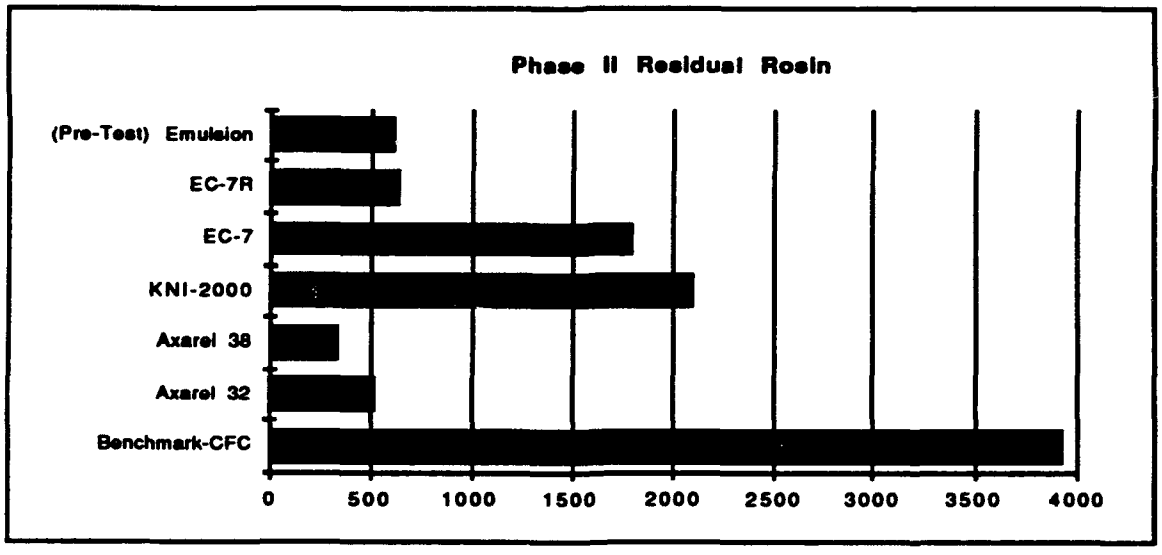

Figure 3.

Preliminary IPC/DOD TR-580 test protocol data is show above in figures 2 and 3 As can be seen, the emulsion process was as good or better than comparable 100% Semi-Aqueous Phase II test results. This data is especially comparable, as the Axarel®-38, Envirosolv® KNI-2000, and Petroferm Bioact® EC7R products were tested in essentially the same batch spray cleaning equipment.

Comparing 5%,20% 100% emulsion cleaning efficiency

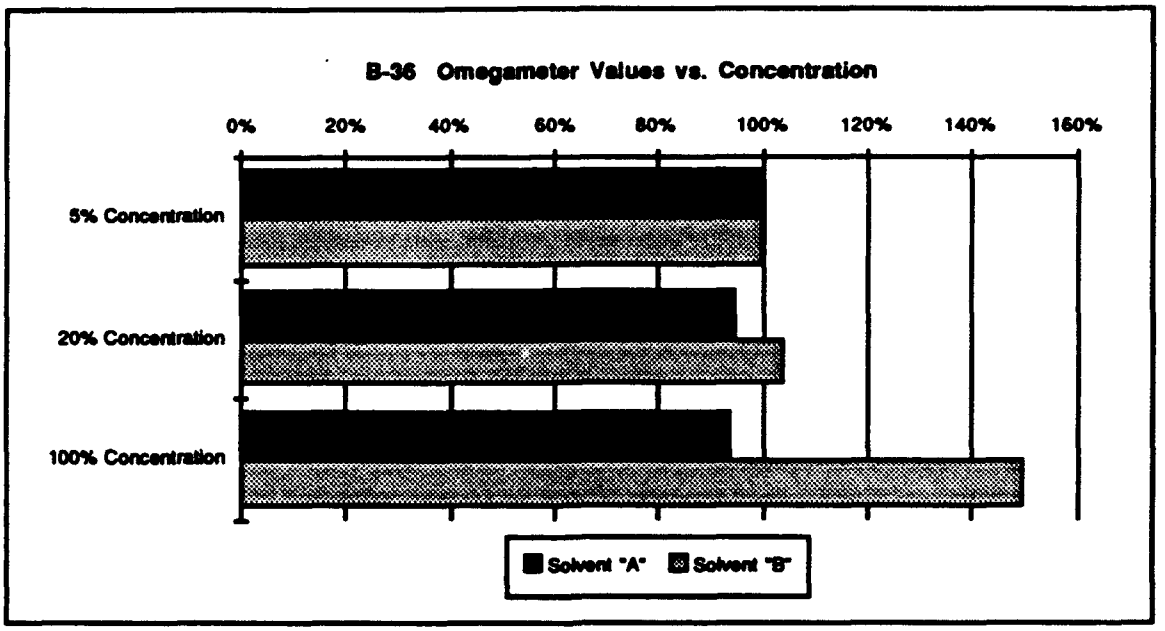

Figure 4.

In order to compare the effect of emulsion concentration on cleaning efficiency, B-36 coupons were wave soldered with RA flux, cleaned and tested. Wash times, rinse times and temperatures were kept the same for the testing. Two solvents were tested. Figure 4 above illustrates the results. For comparison purposes, the data in this fig for the 20 and 100% concentrations was normalized to the 5% Omegameter values. Figure 4 shows that the 5% is very close to the 100% performance of Solvent "A" and is considerably better than the performance of Solvent "B".

Effect of wash and rinse temperature on cleaning efficiency

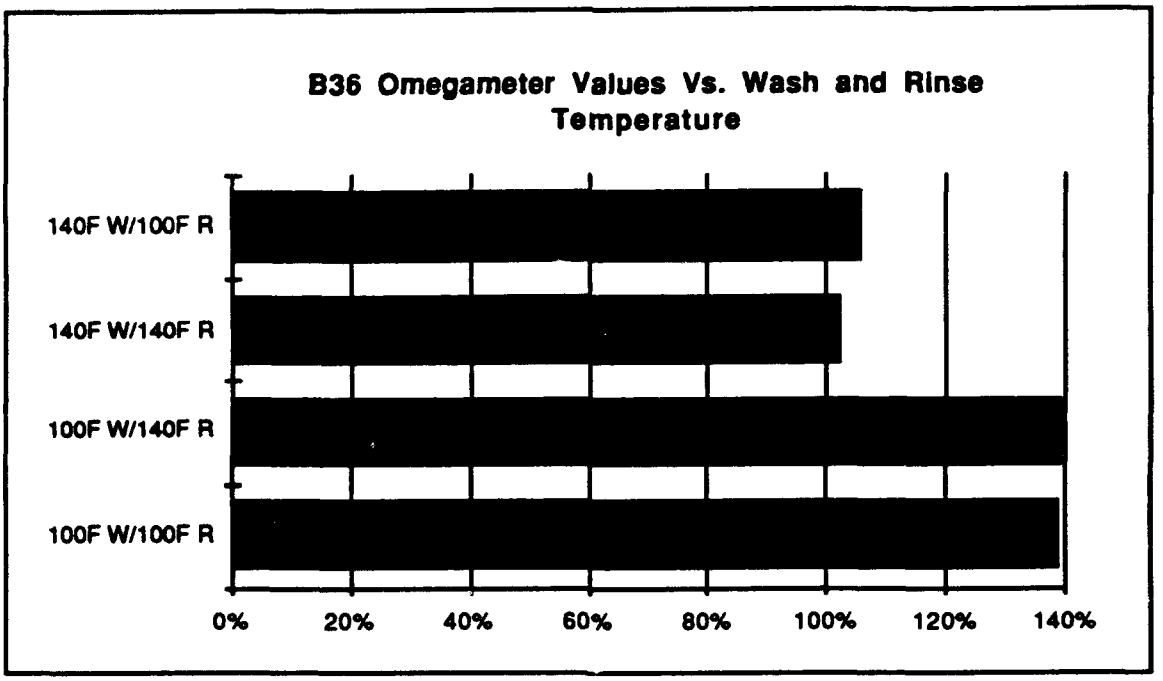

Figure 5.

In order to compare the effect of emulsion wash temperature and water rinse temperature on cleaning efficiency, B-36 coupons were wave soldered with RA flux, cleaned and tested. Wash temperatures for the emulsion were 100F and 140F, rinse temperatures were 100 and 140F also. Wash and rinse times were kept constant at 10 minutes each. Figure 5 illustrates the results. For comparison purposes, Figure 5 data was normalized to the 5% Concentration test Omegameter values.

Equipment and Process

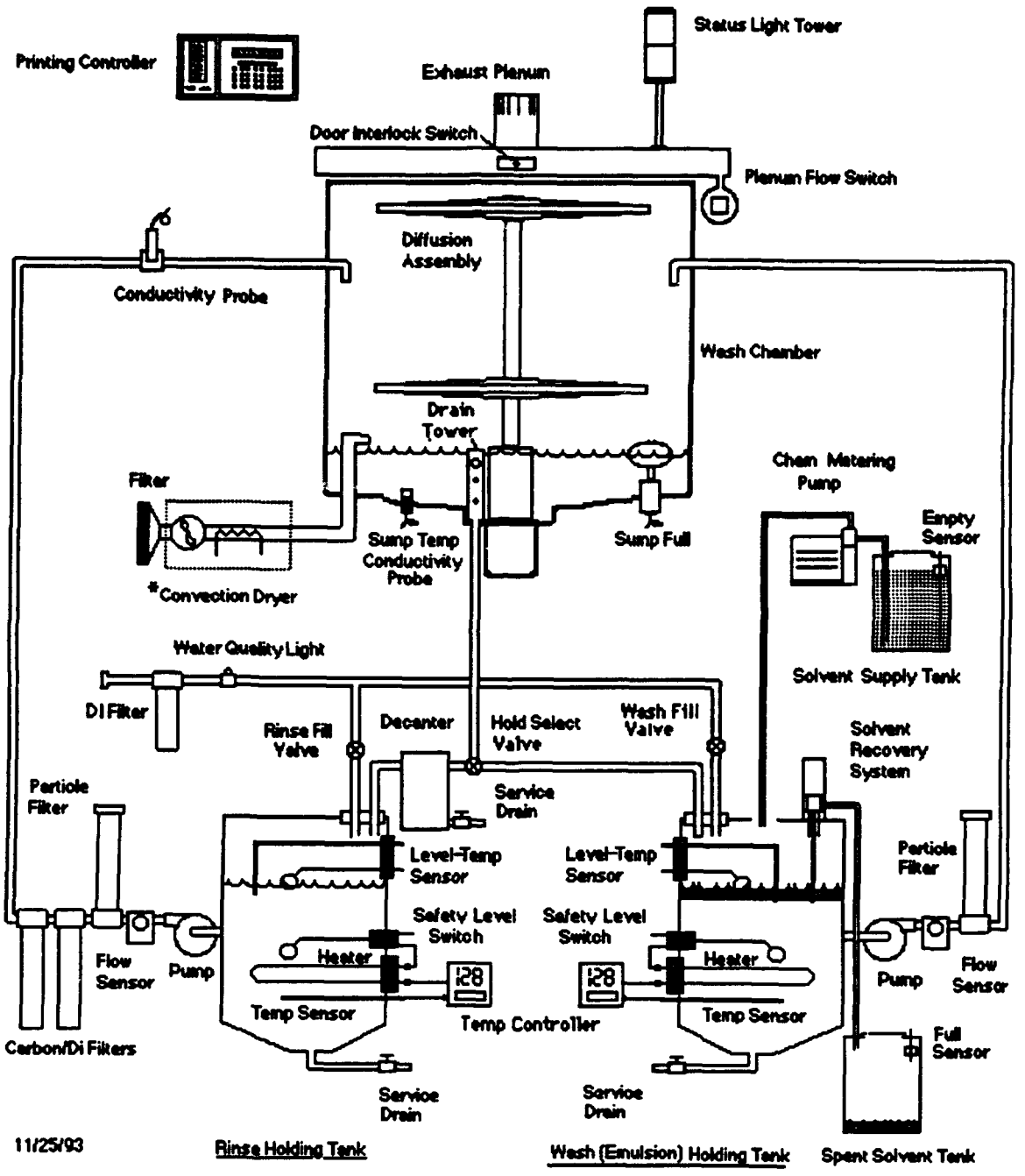

Figure 6.

Equipment and Process (continued)

An implementation of an emulsion cleaning and waste treatment system is shown in figure 6. A typical daily operation sequence would be as follows:

1. Before the first wash of each day, the machine mixes precise levels of new solvent and re-used water, creating a wash solution in the heated wash holding tank, where sensors control temperature and solution levels automatically.

2. During the wash cycle, the wash solution is continually pumped through a particle filter to the wash chamber, and then back to the holding tank, where this closed-loop cycle continues. The solution in the wash chamber is continuously emulsified and recirculated at 60 GPM over the PCB assemblies with a separate pump.

3. After the wash cycle is completed, the emulsion wash solution flows back to the wash holding tank and slowly separates, with the emulsion collecting at the top.

4. During the rinse cycle, water is continually pumped through a particle filter and a series of carbon/DI filters to the wash chamber, through a decanter and back into the holding tank, where this closed loop cycle continues. The rinse water in the wash chamber is recirculated at 60 GPM over the PCB assemblies with a separate pump.

5. After the rinse water is drained from the cleaning chamber, assemblies are automatically dried by a built in dryer. The machine is now ready to continue it's production.

6. At the end of each work day, the machine automatically cleans up the wash solution, removing used solvent to a separate holding tank. The machine is now ready to recharge itself at the start of the next work day.

Conclusions

Controlled emulsion cleaning has many advantages over other cleaning alternatives used for rosin flux cleaning. The process is capable of "Better Than" Phasell cleanliness levels, it provides clean boards with shiny solder joints and has significant waste treatment advantages. The controlled emulsion cleaning process is safer and easier to operate than "Full" Semi-Aqueous. Finally, the controlled emulsion process offers significant cost savings over other rosin removal processes, when cost of waste water treatment is included.

Rex Breunsbach is the founder and currently the President of Electronic Controls Design, Inc., with major responsibility for research and development. He attended Oregon State University School of Electrical Engineering and has had 25 years of experience in the design and manufacture of electronic instrumentation for medical and industrial processes. Earlier work involved development of electronics for the kidney patient hemodialysis machine and the M.O.L.E.® process temperature profiling device. Recent work has focused in the area of batch aqueous, semi-aqueous, and semi-aqueous emulsion closed-loop cleaning systems for electronic assemblies and precision metal parts.

Address: Electronic Controls Design, Inc.
4287-A SE International Way
Milwaukee, OR 97222-8825

ENVIRONMENTALLY SAFE CLEANING PROCESS FOR AVIONICS

BY

Deepak K. Pai

Computing Devices International
3101 E 80th Street
Bloomington, MN 55425-1507
Phone (612) 853-8025

ABSTRACT

This paper describes a Computing Devices International research and development effort to develop environmentally safe soldering and cleaning processes for dense, high performance, circuit card assemblies (CCA) for military avionics. Solder, fluxes, cleaning, and process control will be addressed.

Computing Devices International (CDInt.) has been researching techniques to develop and control environmentally safe soldering and cleaning techniques for surface mount components (SMC) used in military avionics since 1985. We have developed and patented "A Method for Cleaning Process Control" (U.S. Patent No. 4905371, 3/6/90). We have also applied for a patent (8/25/93) on "A Method to Evaluate the Effectiveness of a Cleaning System for High Density Electronics," and submitted several disclosures.

Although CDInt. conducted these research activities primarily to improve the reliability of military avionics, this technology is equally applicable to high performance commercial electronics.

INTRODUCTION

The cleaning of today's high performance and densely populated circuit card assemblies (CCA) designed for avionics is one of the electronic industry's major problems. Chlorofluorocarbon (CFC) and methyl chloroform (MCF) based solvents are currently widely used to clean rosin based fluxes and other contaminants after soldering. Federal legislation(1) has banned the use of solvents containing CFCs, MCFs, and most other ozone depleting substances (ODS) after December 31, 1995. According to one estimate(2), this will require the replacement of more than 150,000 pieces of dedicated cleaning equipment used in the U.S. Pending legislation, higher prices, waste disposal and treatment costs, taxes, and increased environmental awareness have also encouraged the development of environmentally conscious manufacturing processes. Consequently, electronic manufacturers must evaluate and select cleaning processes that are environmentally safe and meet the reliability requirements of their unique products. Cost effective techniques that will evaluate cleaning systems for cleanliness, material compatibility, and long term reliability are in demand.

Since 1989, Computing Devices International (CDInt.), formerly the Government Systems Division of Control Data Corporation, has been developing environmentally conscious manufacturing processes for high density, high performance CCAs.

This paper is an overview of issues pertaining to the cleaning of military electronics.

BACKGROUND

Many of today's environmental problems are caused by manufacturing processes and materials that have been developed over many decades and are still widely used in the military electronic industry. Some of these are: 1) rosin-based fluxes; 2) CFC- and MCF-based solvents; 3) toxic solvents derived from petrochemicals; and 4) solder alloys containing lead.

Prior to the 1987 Montreal Protocol, military electronics manufacturers preferred cleaning solvents containing CFC-113 and MCF in vapor degreasers for rosin flux removal. Various azeotropic blends of these solvents with alcohols increased the efficiency of the process and enhanced the cleanliness of the hardware. The availability of vapor degreasing equipment in various sizes, from small batch units to large-in-line systems, and at relatively lower cost allowed manufacturers to place them at several locations within a plant to optimize process flow.

By December 1995, CFC- and MCF-based solvents will no longer be available, and the electronic industry must choose an alternative. Several producers of CFCs and MCFs have announced accelerated phase outs and production scale-backs. The potential shortages, higher prices, higher taxes, and the possible impact of warning labels on consumer preference have added to the list of reasons to develop and test environmentally safe materials and manufacturing processes.

The technical challenge in developing environmentally safe cleaning processes for high performance electronics has been associated with trends in two major attributes: 1) the dramatic increase in the functional density and decrease in the electronics feature size; and 2) the large number of alternatives available for cleaning assemblies.

During the past ten years, there has been consistent, exponential, annual growth in the density of printed wiring boards and substrates (grid density). Grid density is expressed as the sum of one line width, two spaces, and one via diameter.

The trend in the grid density and range of application of various packaging technologies is shown in figure 1. The advances in interconnect density increase the integration and speed of the integrated circuits (IC) thereby reducing the size, power, and cost for a given function. The substrates used on the Multichip Modules (MCM) provide very high grid density.

The trends in component feature size are shown in figure 2. The component pitch decreased from .100 inch for the 1960's dual in-line packages to .004 inch for the modern Very Large Scale Integrated circuits (VLSI).

The range of application of various components and corresponding Printed Wiring Board (PWB)/substrate technologies are shown in figure 3. The thru hole PWB designs typically use components with large (.100 inch) pitch and low-lead-count components. The surface mount PWBs and MCM substrates, on the other hand, use relatively smaller pitch and high-lead-count components.

Densification and miniaturization have also introduced several new materials and components. Therefore, it is necessary to study trends in design, new materials, and material compatibility when evaluating and testing cleaning chemicals and cleaning systems.

Industry surveys indicate that a large number of ODS-free alternatives are available. However, there is not one product that meets all the requirements of electronics manufacturers. During the late 1980's, manufacturers evaluated other solvent base materials, such as hydrogenated CFCs (HCFC), which can be used in existing vapor degreasing systems with minor modification. Unfortunately, these solvents still have ozone depleting potential and are toxic. EPA and OSHA regulations must also be followed for manufacturing plant and environmental compliance. It is very important to select the cleaning chemicals and processes that will be considered environmentally safe well beyond the year 2000.

MAJOR CLEANING ISSUES

The major cleaning issues facing manufacturers of military avionics are: 1) choice of fluxes; 2) cleaning chemicals; 3) cleaning equipment; 4) material compatibility; and 5) material handling. These are discussed briefly in the following paragraphs.

Military electronics manufacturers are required to use rosin base fluxes in accordance with MIL-STD-2000 and other applicable specifications. Military specifications are being revised to allow use of aqueous, low-residue and no-clean fluxes. Various chemistries available to clean rosin flux residues after soldering CCAs are:

> ***AQUEOUS*** - The aqueous cleaning process uses saponifiers to render rosin flux residues water soluble. The water, mixed with saponifier, also removes other non-ionic and ionic contaminants. Additional process steps are required to rinse the CCA with deionized water and blow dry.
>
> ***SEMIAQUEOUS*** - The semiaqueous cleaning process uses a solvent to dissolve rosin flux residues from the CCA. This process requires additional process steps to rinse the solvent with deionized water and blow dry.

In both cases, the contamination laden solvent/water is flushed from the parts by rinsing with water. A need exists to provide a method of removing the rinse water from the small (.002 inch or less) gaps. In addition, these methods do not remove small (.0002 inch or less) particulate effectively. This may cause reliability problems with high density, high reliability military modules and MCMs.

Commercial electronics manufacturers have used aqueous fluxes for many decades. The flux residues can be easily cleaned using an aqueous cleaning system and surfactants. These cleaning systems are relatively less expensive compared to the semiaqueous systems. The aqueous and semiaqueous cleaning equipment may require a closed-loop recycling system if direct-to-drain discharge is not allowed by state and local authorities. Deionized water dissolves the lead in the lead/tin solder alloys, which can be separated by using chelating ion exchange resin. The semiaqueous cleaning system also needs a separator to separate solvents from the water. These solvents need to be replaced after reaching certain contamination saturation levels. Transportation of the hazardous waste solvents may be expensive.

No-clean fluxes have been used for many years by manufacturers of low cost consumer electronics. Soldering is performed using controlled atmosphere to reduce oxidation. The CCAs are not cleaned after soldering. The no-clean flux residues often interfere with subsequent probe testing. It is possible to clean these residues using aqueous cleaning.

The high reliability, high-performance military modules and MCMs often use expensive state-of-the-art PWBs/substrates and fine-pitch, high-lead-count VLSIs. These assemblies often use adhesives with high thermal conductivity and encapsulants/coatings for

environmental protection. The fluxes and the cleaning chemicals, including deionized water, must be compatible with these materials for long term reliability. Some of the conformal coating delamination and CCA corrosion problems discovered during environmental testing can be easily traced to material handling. In spite of solvent and deionized water cleaning, inspection, and contamination testing in accordance with MIL-STD-2000, finger prints on components and PWBs often show up underneath the conformal coating during humidity test. In the past, the use of aggressive cleaning solvents after assembly has covered up most of the material handling problems. These solvents will be replaced by new, relatively less aggressive chemicals and water. New assembly processes will force manufacturers to narrow the process windows. Keeping ionic and non-ionic contamination at a minimum at all stages of procurement and manufacture will be critical to achieving long term reliability.

CLEANING PROCESS CONTROL

Electronics manufacturers are scrambling to evaluate and select cleaning chemicals, equipment, and processes that are environmentally safe, while meeting the requirements of their unique products. A number of environmentally friendly/safe processes that claim effectiveness in cleaning CCAs are available. Cost effective techniques that assess cleaning systems for cleanliness and long-term reliability are needed.

CDInt. has been researching techniques to develop and control environmentally safe cleaning processes for high performance military electronics (3,4,5) since 1989. Internal research has produced two assessment techniques: 1) A Method for Cleaning Process Control, D. K. Pai, U.S. Patent No. 4905371, 3/06/90; and 2) A Method to Evaluate Effectiveness of a Cleaning System for High Density Electronics, D. K. Pai, et. al., patent pending. These testing techniques, which do not subject actual production-run CCAs to possible contamination are described in the following paragraphs.

GLASS SUBSTRATE

In this technique, the surface layer of a PWB or a high-density MCM substrate is deposited on transparent Pyrex glass. The electrical components are attached to the surface layer pads on the glass using the appropriate process for the soldering and selected adhesives. After attaching the components, the glass substrate is cleaned. Then, the effectiveness of the cleaning system is evaluated by inspecting the glass substrate from both sides without removing the components. The glass substrate can also be subjected to humidity and surface insulation resistance (SIR) testing to evaluate the cleaning system for material compatibility, corrosion, and long-term reliability. The glass substrate can also be used to optimize process parameters (e.g., conveyor speed, spray pressure and direction, temperature, and drying) of an existing cleaning system for a new product.

The glass substrate technique being used to evaluate new cleaning processes is shown in figure 4. The back side of this glass board, showing contamination between VLSIs and the glass, is shown in figure 5. Figure 6 shows 4.5 x 4.5 inch glass boards with an avionics

CCA pattern. A glass board with high density (.003 inch line/space) circuit pattern is shown in figure 7. Characteristics of typical test substrates are shown in Table 1.

TABLE 1: Typical Test Substrate Characteristics

Size	.25 x .25 to 12.0 x 12.0 inch .25-inch thick Pyrex glass
Conductor Material	Copper
Minimum Feature Size	.001 inch wide pad, .001 inch space
Surface Layer	Solder, nickel, copper, or gold

4-PI PATTERN

The 4-Pi pattern is a circuit with four comb patterns, in four directions, electrically connected to each other. The 4-Pi pattern is used to fine-tune the direction of spray nozzles in a cleaning system. The pattern can be incorporated in the surface layer artwork, or used with two parallel plates for SIR testing. CDInt. can fabricate the 4-Pi pattern with a minimum feature size of .001 inch wide line and .001 inch space on Pyrex glass. Figure 8 shows a .4 inch by .4 inch 4-Pi pattern with .005 inch wide line and .005 space.

PIE COMB PATTERN

The pie comb pattern, shown in Figure 8, has conductors arranged with variable spacing in a radial direction. The spacing is minimum (.001 inch) near the center of the pie. This pattern is used to evaluate the capability/limits of a cleaning system to clean the smallest gap between two conductors. Similar to the 4-Pi pattern, this pattern can be incorporated in the surface layer artwork, or used with two parallel plates for SIR testing.

PARALLEL GLASS PLATES

This device provides a cost-effective technique to evaluate and control a cleaning process. CDInt.'s unique 4-Pi pattern (patent pending) is on one of two plates. Spacing between the plates can be adjusted to range from .002 inch to .050 inch. Figure 9 shows a parallel glass plate with the 4-Pi pattern. The technique involves first applying flux to the gap between the plates. Then the device is baked to dry the flux. After cleaning, an inspection is performed and a humidity or SIR test may be conducted. Figure 10 shows a 4-Pi pattern during SIR test.

SUMMARY

A large number of cleaning systems that claim environmental safety and effectiveness in cleaning CCAs are available in the market. However, considerable development and process refinement have yet to be done to apply these technologies to high-density, high-performance, military modules with fine-pitch, high-lead-count components. Computing Devices International's glass substrates, which have integrated, customer test patterns, facilitates -- and have already demonstrated the environmental safety and effectiveness of -- the required process evaluations and subsequent control techniques.

REFERENCE

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3. Deepak K. Pai and Gene A. Maday, "An Innovative Approach to Control Cleaning Process", Computing Devices International Publication, November, 1992.

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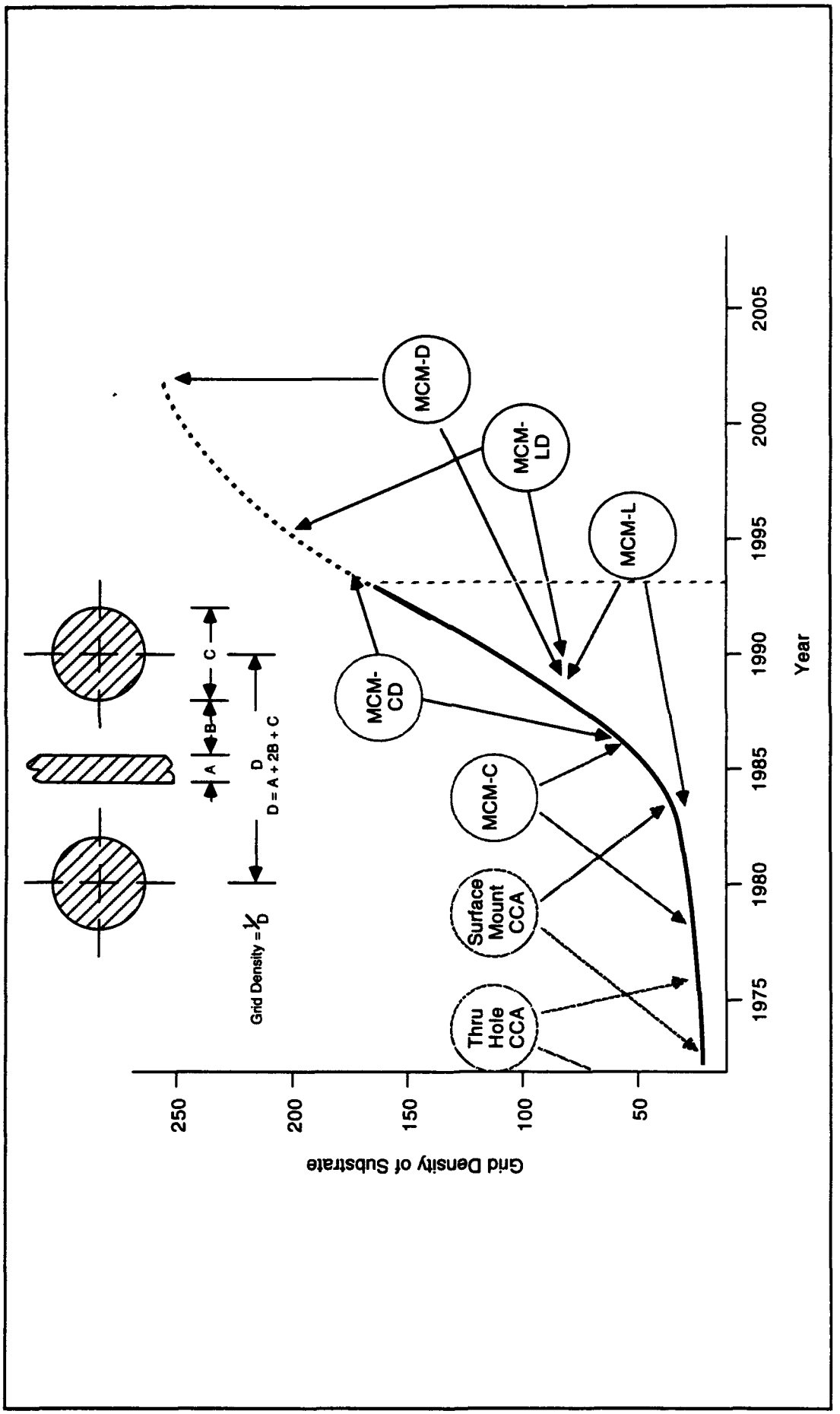

Figure 1. Range of Application of Various Packaging Technologies and Substrate Grid Density

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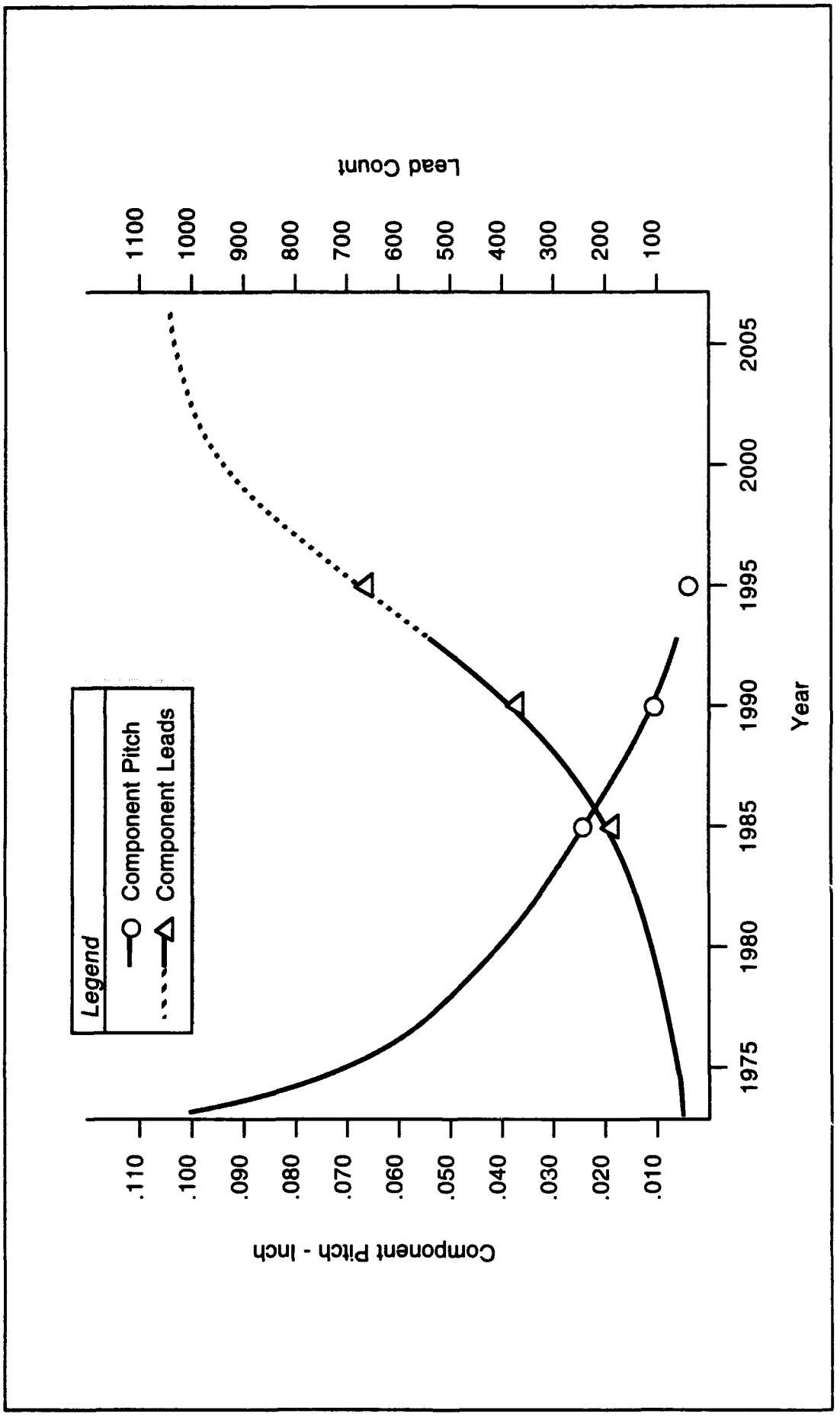

Figure 2. Technology Trends – Component Feature Size

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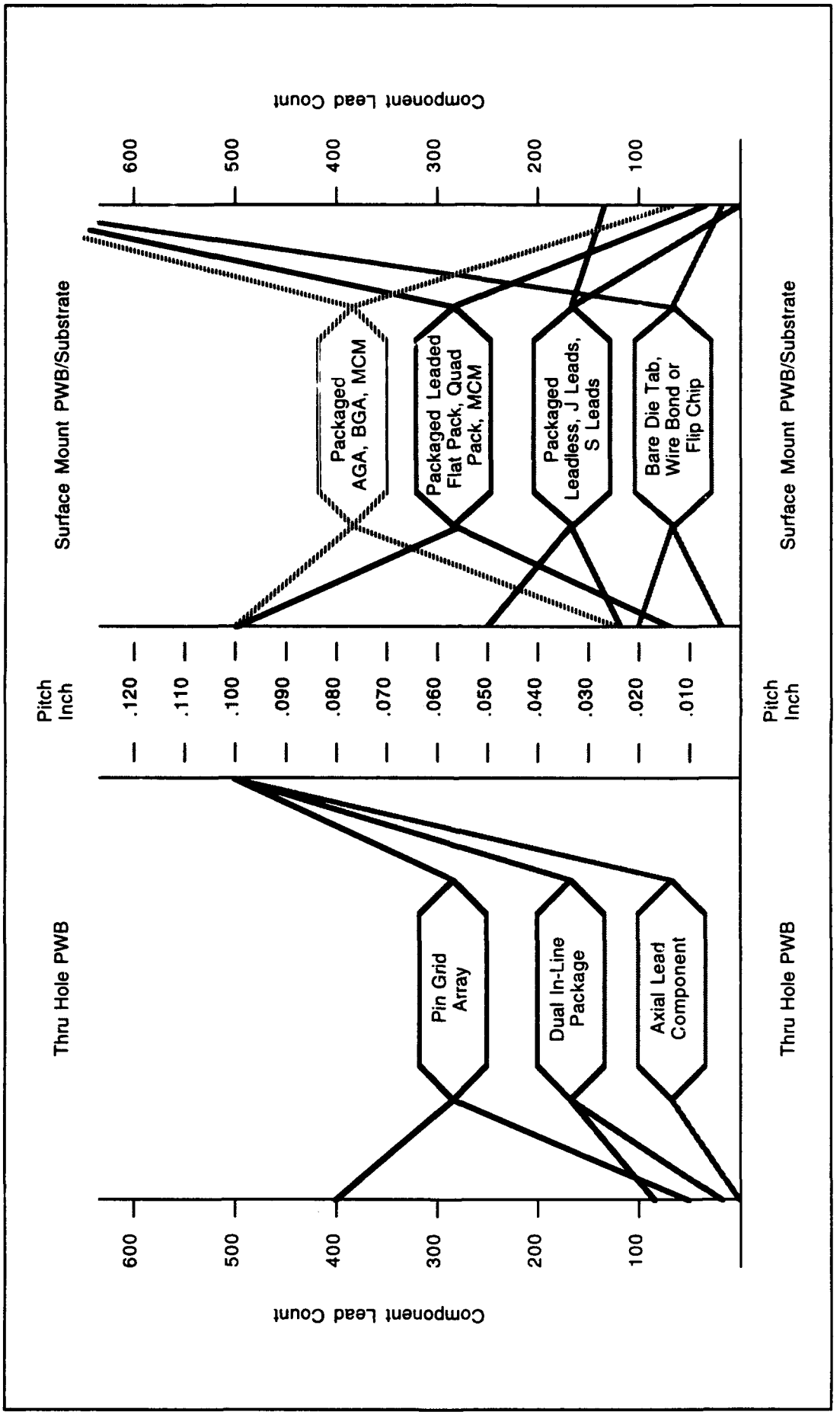

Figure 3. Range of Application of Various Components and PWB/Substrate Interconnect Technologies

RCR-1607(4)

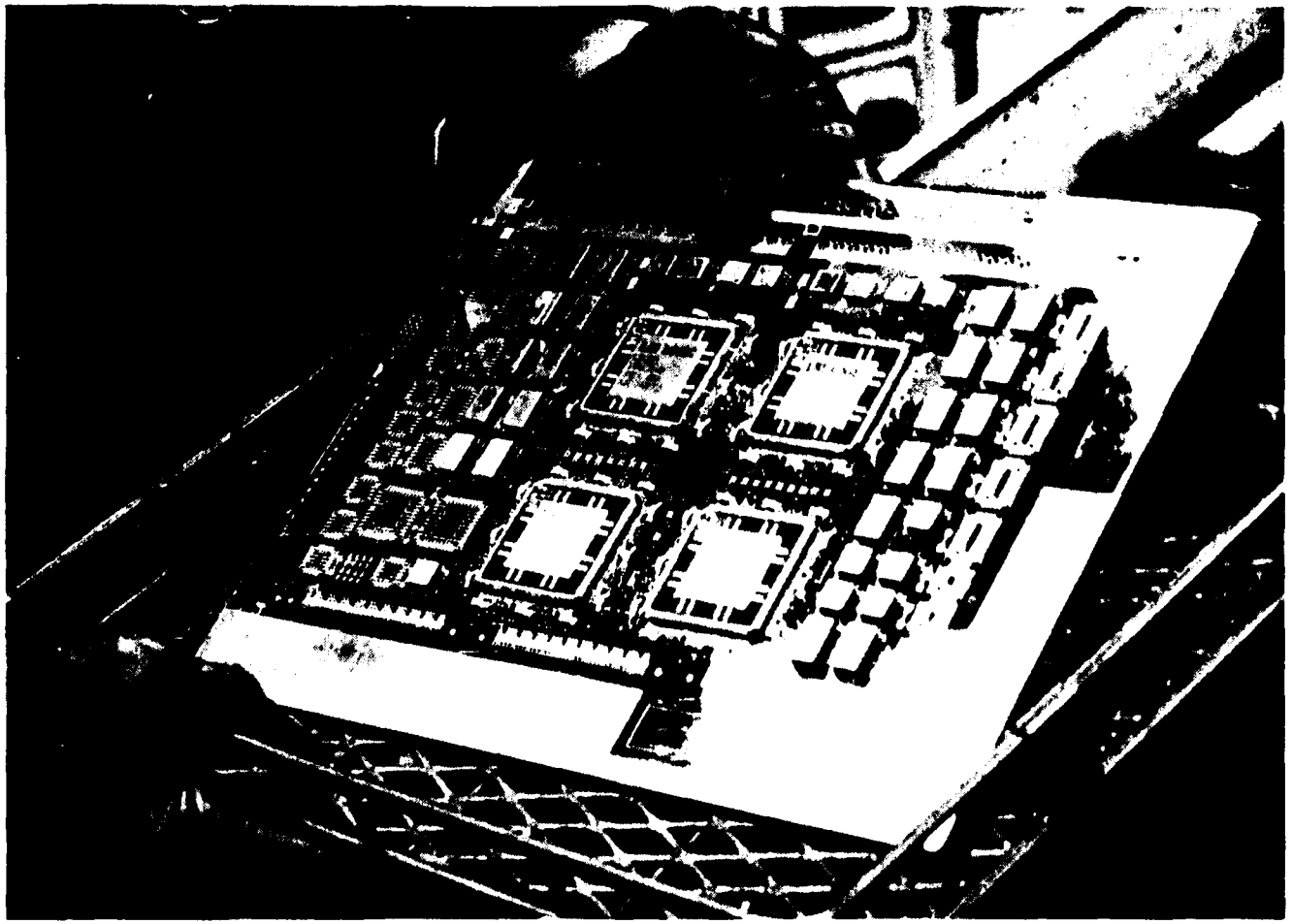

Figure 4. A 6 x 9-Inch Avionics Module Pattern on Glass With Four VLSI Packages Soldered to Optimize Cleaning Process Parameters

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Figure 5. Back Side of the Glass Board in Figure 6 Showing Contamination (Arrows) Between VLSI and the Glass

RCR-1607(7)

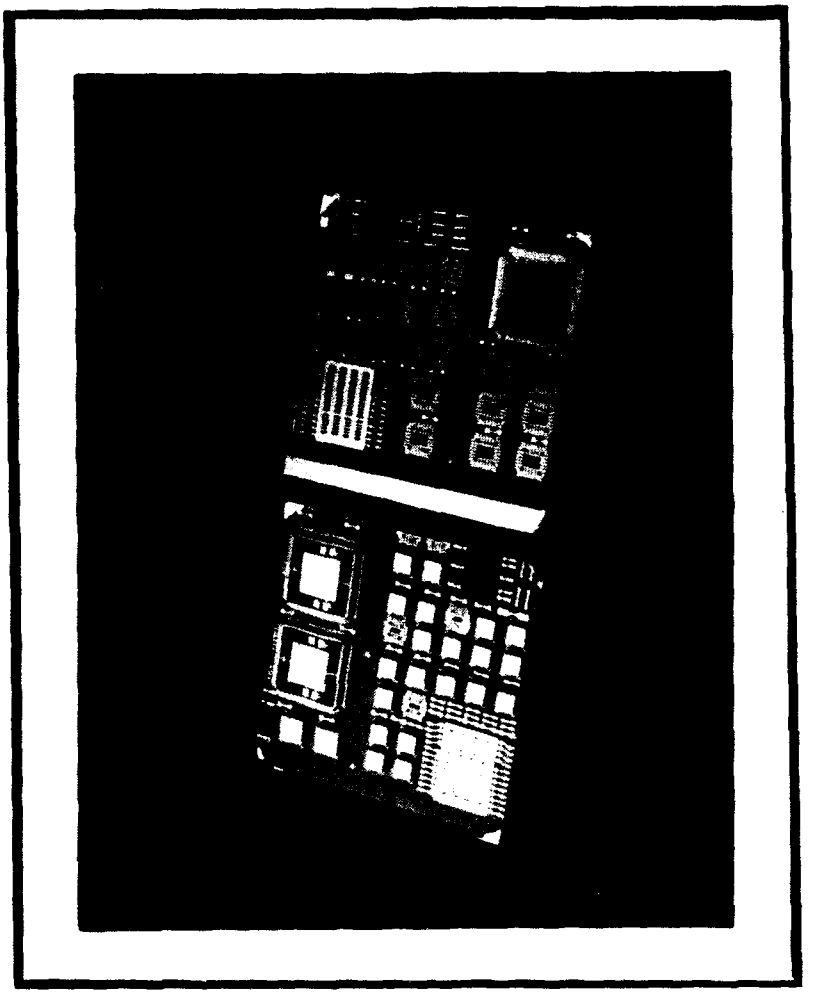


Figure 6. Avionics Module Pattern on 4.5 x 4.5-Inch Glass

RCR-1607(13)

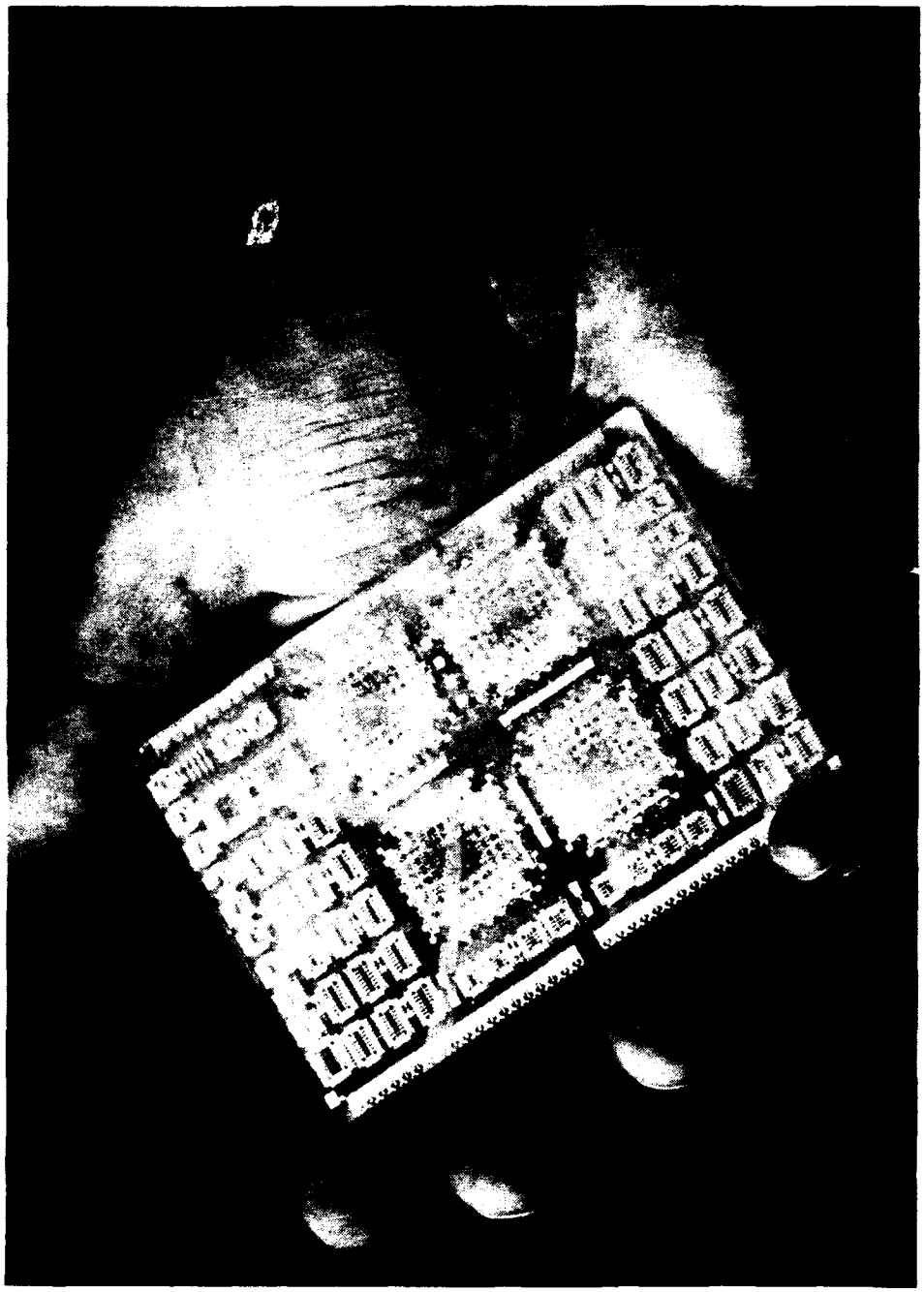
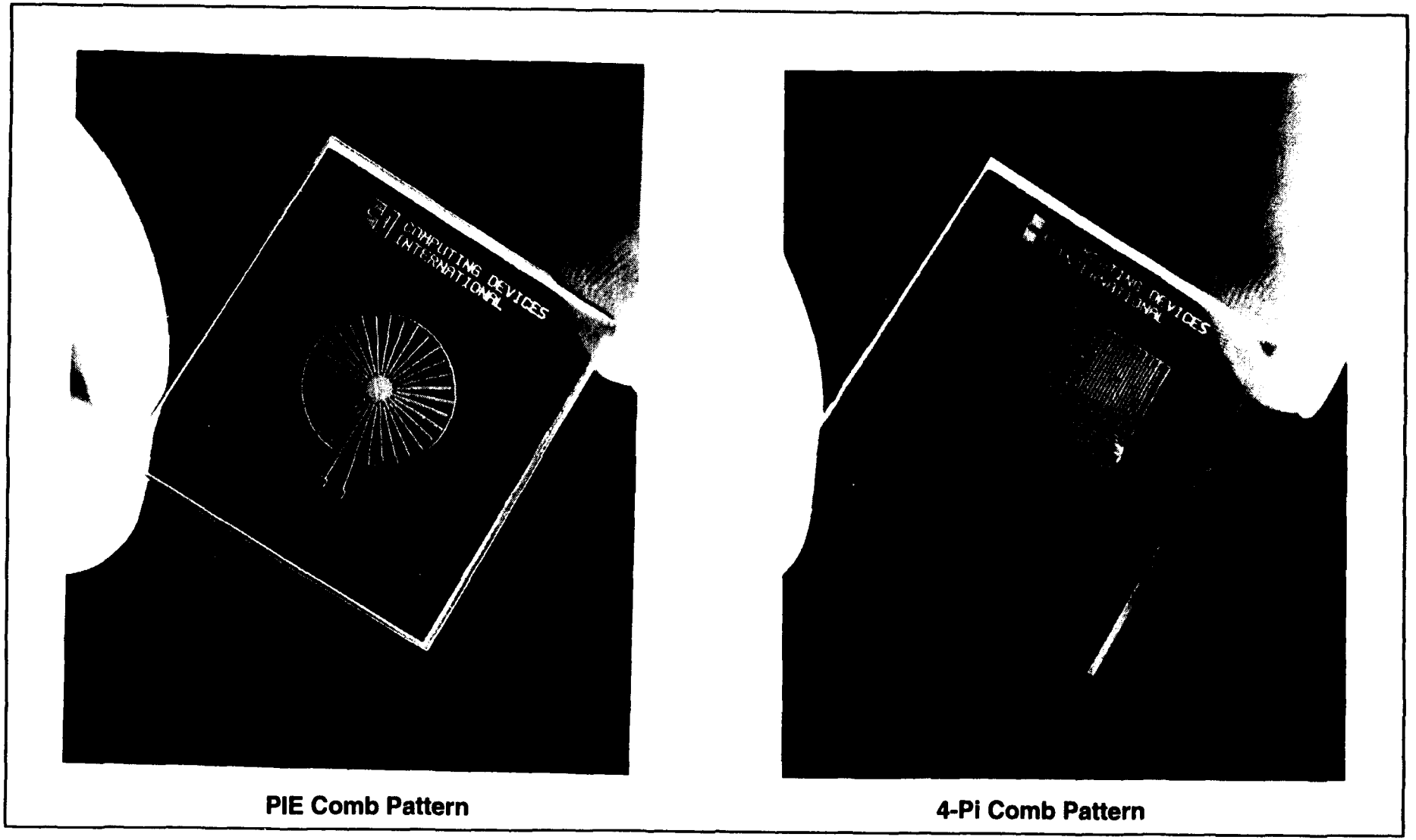


Figure 7. A Glass Board With High Density (.003 Inch Line/Space) Circuit Pattern

RCR-1607(8)



PIE Comb Pattern

4-Pi Comb Pattern

Figure 8. Comb Patterns to Test Surface Insulation Resistance

RCR-1607(9)

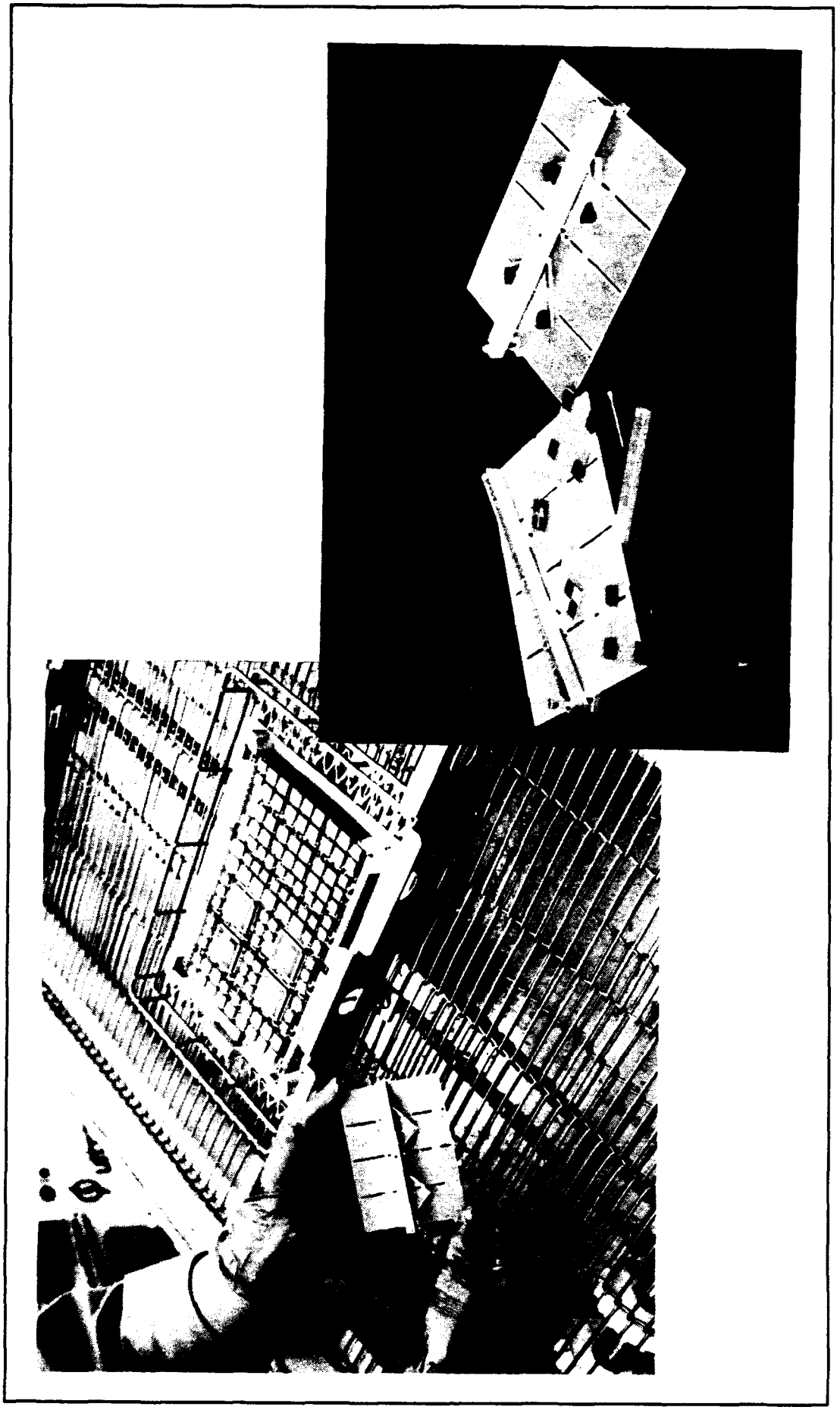


Figure 9. Parallel Glass Plate With 4-Pi Pattern

RCR-1607(10)

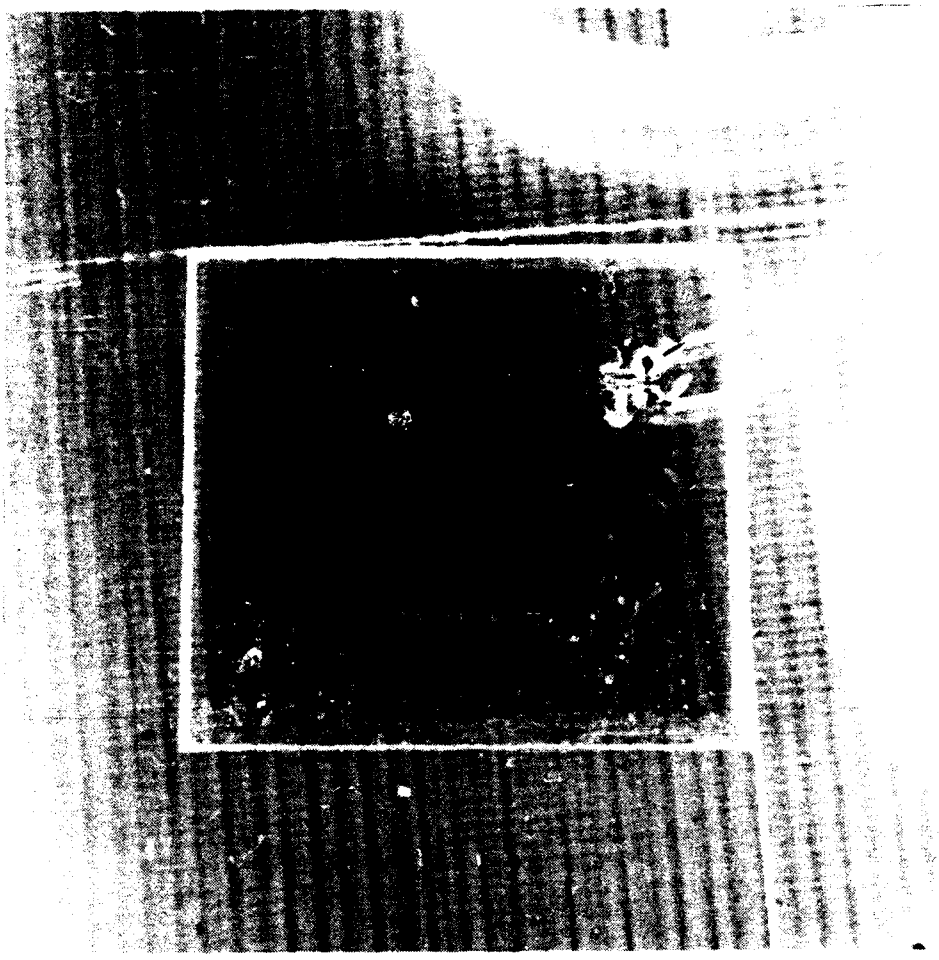


Figure 10. A 4-Pi Comb Pattern During SIR Test

RCR-1607(11)

Deepak K. Pai is a Technical Consultant at Computing Devices International. He has had 24 years of experience in military electronics and 4 years of experience in thin film technology. He is the author of several publications in electronics technology, holds two U.S. patents, and has seven patents pending.

Deepak holds a Bachelor of Engineering degree in ME, a Master of Technology degree in ME, and a Master of Science degree in IE/OR.

Address: Computing Devices International
3101 E. 80th Street
Bloomington, MN 55425-1502

SOLDER JOINT DURABILITY--DESIGN IMPLICATIONS FROM FINITE ELEMENT MODELING AND EXPERIMENTAL TESTING OF A CERAMIC GULL WING PACKAGE

by

S. L. Appl, K. L. Coates, M. Rassaian, and D. M. Rose
The Boeing Company
Seattle, Washington

ABSTRACT

Since durability analyses are becoming more critical in the design of military electronics, a thorough understanding of solder joint reliability and the ability to accurately model and predict solder joint reliability are essential. This paper describes a statistically designed experiment (DOE) conducted to obtain thermal shock (-55 to +125 C) reliability data for an 84 I/O, 50 mil pitch , ceramic package mounted on a glass-reinforced epoxy (FR-4) printed circuit board. These materials, the ceramic and the FR-4, provided a test case with significant thermal mismatch. Since the compliance of leaded surface mount devices has also been widely shown to affect the thermal fatigue life of the solder joints, four different gull wing lead bend configurations were compared. Both leg height and shoulder length were varied. In addition, the effects of two different soldering processes, vapor phase and hot bar, were evaluated.

Experimental fatigue life results which include the number of cycles to first electrical failure and visual observations of crack propagation are presented. A statistical analysis of the test data is provided. In order to analytically predict fatigue life, a nonlinear finite element analysis is performed for the selected lead geometries. Comparison of the experimental data and the analytical fatigue life predictions serves to validate the analytical approach.

INTRODUCTION

Thermal fatigue caused by thermal expansion mismatches between materials connected by a solder joint is a major threat to the mechanical integrity of the solder joint. Often, accelerated environmental tests are performed to verify sufficient solder joint reliability for a specific application. However, such tests

are typically expensive and time consuming. As a valuable supplement to thermal shock or thermal cycling tests, finite element analyses can be performed to compare and verify electronics hardware design choices. As the density in current designs continues to increase, and thus the number of failure opportunities steadily increases in today's complex systems, the ability to ensure solder joint durability becomes even more essential. Analytical life predictions based on finite element analyses provide a powerful tool to ensure solder joint durability; however, they can be used with even greater confidence when validated by comparison with experimental results.

In this experiment, a ceramic gull wing package mounted on a glass-reinforced epoxy (FR-4) circuit board was used as the test vehicle, since these materials provided a case with significant thermal mismatch. Since the compliance of the leads is also known to affect the solder joint reliability, four different gull wing lead bend configurations were compared. Both leg length and shoulder length were varied. In addition, the effects of two different soldering processes, vapor phase and hot bar, were evaluated. A statistical analysis of the experimental data was performed. A three-dimensional nonlinear finite element model was used as the basis for analytical fatigue life predictions. Finally, the experimental and analytical results for the thermal fatigue life are compared.

EXPERIMENT DESIGN AND PROCEDURES

An experiment was designed to determine the effect of three treatment factors on solder joint reliability during thermal shock testing. The three factors each have two levels as shown in Table 1, giving a total of eight treatment combinations (2 x 2 x 2). Each treatment occurs with all combinations of the other factors giving rise to a full factorial design. Five replicates were fabricated for each treatment combination giving a total of 40 samples. Two of the variables, leg length and shoulder length, are defined in Figure 1.

TABLE 1. Experiment Variables

Treatment Variable	Levels	Code
Soldering Method	Vapor Phase/Hot Bar	V, H
Leg Length	Long/Short	L, S
Shoulder Length	Long/Short	L, S

The samples consisted of a top brazed ceramic gull wing package which had 84 leads on 50 mil pitch. The leads were made of Alloy 42 plated with a

minimum of 60 micro inches of gold and were 0.010" thick by 0.018" wide. The inner lead pads were wire bonded with gold in a daisy chain pattern corresponding to the pattern on the circuit board to allow for continuous electrical monitoring during thermal shock testing.

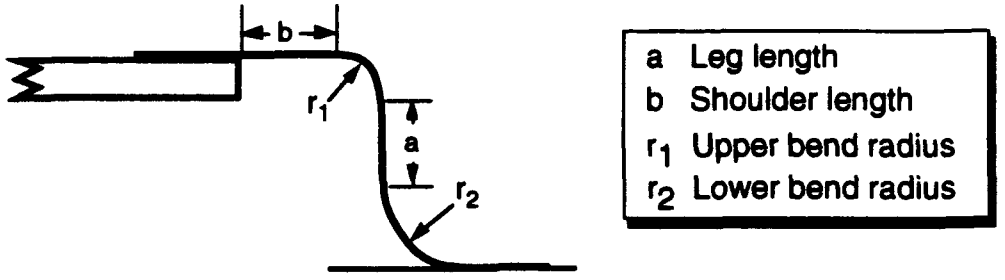


FIGURE 1. Gull Wing Lead Geometry Parameters

The packages were soldered to 2.75"x 2.75", 0.090"-thick glass-reinforced epoxy (FR-4) circuit boards. In order to provide solder for the solder joint connection on the hot bar samples, the printed wiring boards (PWBs) had an additional 1 mil of plated solder beyond that which is deposited in the standard PWB manufacturing process. The PWBs for the vapor phase samples did not have the extra plated solder. The pad dimensions were 0.030" x 0.150".

The lead geometries, shown in Table 2 , were chosen to provide various lead compliance values and thus various thermal fatigue lives. The spring constant, K_D, is the diagonal flexural stiffness of an unconstrained, corner-most lead. The spring constants were calculated using equations derived by Kotlowitz [1]. Figure 2 depicts the relationship between the leg and shoulder lengths and the spring constant of the lead. To obtain the desired geometries, the leads were bent using a single sided forming system. The leg lengths were set using a machine adjustment, and a shim was used to obtain the longer shoulder lengths. The values shown in Figure 2 are average dimensions based on measurements of the formed leads made with an optical measurement system. Prior to forming the leads, the parts were tinned in a flowing solder pot.

For the vapor phase samples, a standard 63/37 SnPb (88% metal content) solder paste with RMA flux was used. The paste was applied using an 8-10 mil thick brass stencil and a rubber squeegee. The samples were soldered in a dual vapor phase reflow system.

TABLE 2. Lead Geometry/Compliance

Treatment (Leg/Shoulder)	Leg Length (a)	Shoulder Length (b)	Upper Bend Radius (r_1)	Lower Bend Radius (r_2)	Spring Constant, K_D (lb/in)
Long/Long	0.042	0.111	0.012	0.022	33.1
Long/Short	0.034	0.075	0.015	0.026	47.6
Short/Long	0.018	0.110	0.012	0.019	66.5
Short/Short	0.017	0.074	0.014	0.020	99.6

(All dimensions in inches. Standard Deviation = 0.002 in.)

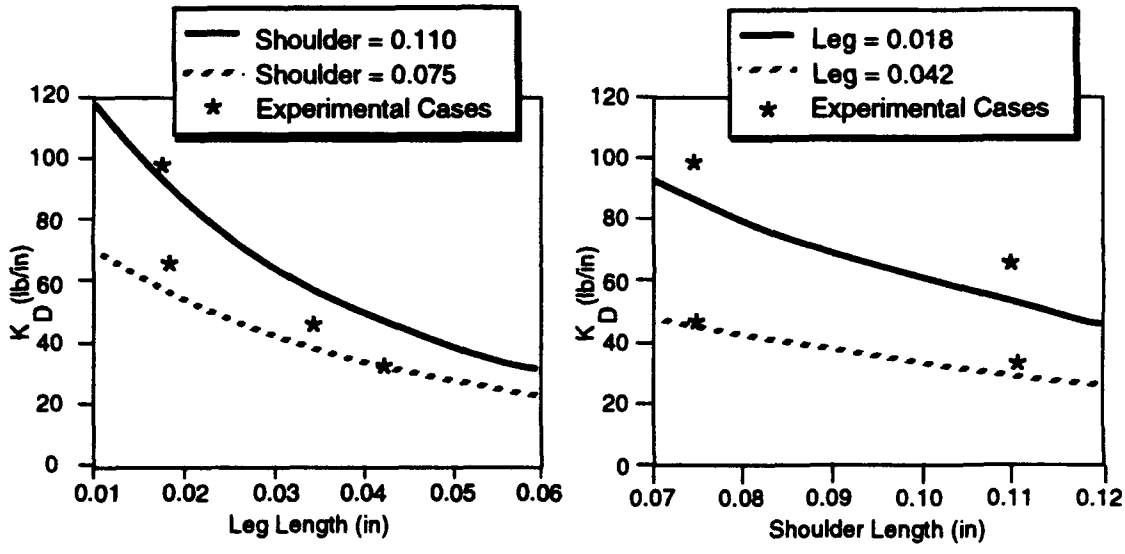


FIGURE 2. Spring Constant as a Function of Lead Geometry

The remaining printed wiring assemblies (PWAs) were hot bar soldered using a single sided blade. As mentioned earlier, the PWBs for hot bar soldering had one mil of additional plated solder on the pads, and no additional solder was applied at this point. A bond temperature of 300 C and a pressure of 6.3 pounds was applied for 4 seconds. The blade was leveled prior to the first and third side being soldered on each sample and was cleaned prior to soldering each side. The first side soldered was the side with pin #1 and soldering continued counter clockwise thereafter. All samples were assembled in a randomized order to avoid systematic errors.

Due to the two different methods of solder application, significantly different volumes of solder were achieved in the vapor phase soldered joints and the hot bar soldered joints. Figure 3 shows a typical vapor phase joint which has considerably more solder volume than a representative hot bar joint shown in Figure 4.

FIGURE 3. Typical Vapor Phase Solder Joint (High Volume)

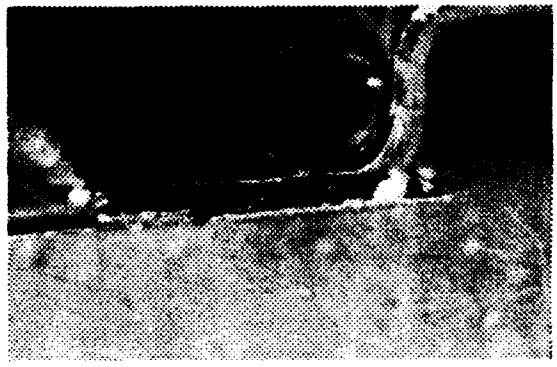


FIGURE 4. Typical Hot Bar Solder Joint (Low Volume)

The thermal shock test used was a variation of MIL-STD-883, Method 1011.3. The PWAs were subjected to cycling between -55 and +125 C with 30 minute dwell times. The chamber used was an air-to-air rotary thermal shock chamber, and the chamber air temperature recovery time was less than 2 minutes.

The electrical continuity of each sample was monitored continuously during thermal shock using an event detector. The system is configured to detect opens (>1000 ohms) as short as 0.2 microseconds. All of the PWAs were tested to failure, i.e. until the resistance exceeded 1000 ohms for longer than 0.2 microseconds.

Visual inspection of the samples was performed prior to thermal shock testing and periodically during testing. Inspection was performed by one inspector with a microscope at 20X. Any visible cracks in the joints were recorded. In order to classify the observations, four crack categories were established (Table 3). These categories were based on the worst side of the joint. Figure 5 shows a representative cracked joint (Crack score = 3).

TABLE 3. Crack Score Categories

Crack Score	Observed Crack Length
0	No Crack
1	0-25% of foot length
2	25-50%
3	50-100%

FIGURE 5. Representative Solder Joint Crack

EXPERIMENT RESULTS AND STATISTICAL ANALYSIS

Electrical Failure Data

The primary response measurement was thermal shock cycles to electrical failure. The individual electrical failure values are shown in Figure 6, with the small squares representing the vapor phase results and the x's representing the hot bar results. The treatment means with 95% confidence limits are given by the diamonds where the horizontal line represents the mean, and the top and bottom points of the diamonds represent the upper and lower bounds. The circles to the right graphically provide information for all paired comparisons of the treatments. The Tukey-Kramer [2] procedure was used in making all paired comparisons while controlling the simultaneous significance level. Treatment combinations are significantly

different if their corresponding circles in the right of the figure do not intersect. Comparing the means, it is seen that vapor phase with long leg length and long shoulder length, VLL, is the top performer. It has a significantly greater lifetime than six of the other seven combinations, as indicated by the circles on the right. The two best treatment combinations, VLL and VLS, are not significantly different from each other, as shown by the overlap of their circles. The treatment averages are also listed in Table 4.

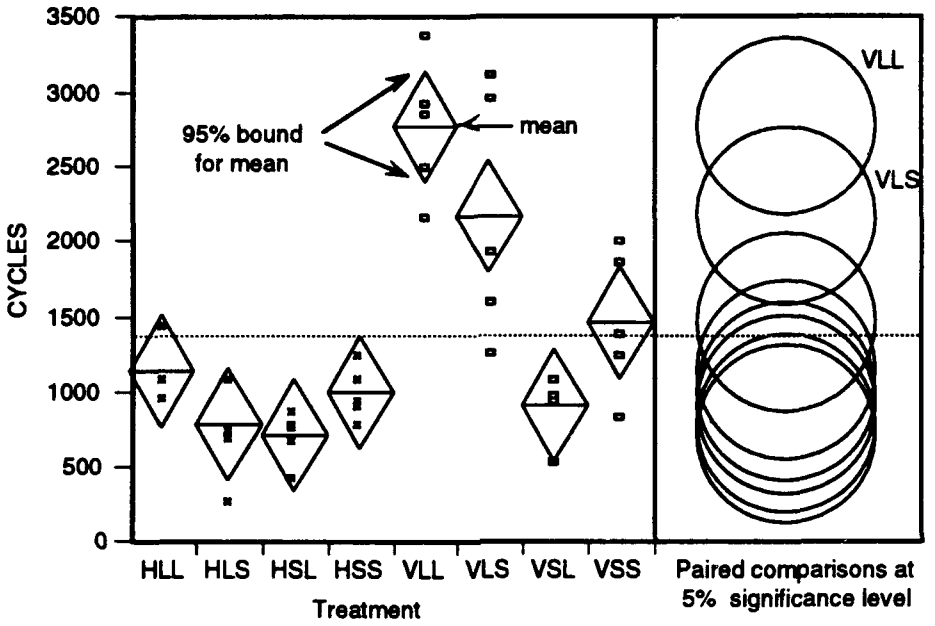


FIGURE 6. Mean Lifetime by Treatment Combination (Number of Cycles to First Electrical Failure)

The analysis of variance (ANOVA) results in Table 5 provide an assessment of the effect of the different treatments. The single most significant factor is the solder technique, as indicated by the large sum of squares (amount of variation attributable to this factor) and the F ratio. If there were no solder effect, the chance of getting this large an F value is less than .0001, as indicated by the last column. The leg length had the next largest sum of squares and was highly significant. In addition to the significance of these two main effects, there is also a significant interaction between them. Figure 7 shows the pairwise interaction of the main factors. The significant interaction between solder technique and leg length is shown in the middle plot in the top row where the two lines have different slopes. In other words, vapor phase and long leg length work better together (longer life) than predicted solely by the main effects alone. In contrast, no interaction

between solder technique and shoulder length is seen in the right hand plot in the top row where the lines are parallel. The other significant interaction between leg length and shoulder length is shown by the crossing of lines in the middle chart in the bottom row. Although this interaction is statistically significant, shoulder length has a considerably smaller impact on solder joint life, as seen in the two top treatment combinations in Figure 6.

TABLE 4. Mean Lifetime by Treatment Combination (Number of Cycles to First Electrical Failure)

Mean Estimates

Treatment	Number of Replicates	Mean	Std Error of Mean
HLL	5	1137.2	186.3
HLS	5	780.2	186.3
HSL	5	707.8	186.3
HSS	5	998.4	186.3
VLL	5	2769.6	186.3
VLS	5	2172.8	186.3
VSL	5	910.4	186.3
VSS	5	1467.8	186.3

TABLE 5. ANOVA Tests of Main Effects and Their Interactions

Analysis of Variance

Source	DF	Sum of Squares	F Ratio	Prob>F
Solder	1	8,542,381	49.2	<0.0001
Leg	1	4,814,278	27.7	<0.0001
Solder*Leg	1	3,460,381	9.9	0.0001
Shoulder	1	6,996	0.0	0.8421
Solder*Shoulder	1	455	0.0	0.9594
Leg*Shoulder	1	2,029,052	11.7	0.0017
Solder*Leg*Shoulder	1	16,0402	0.9	0.3435
Error	32	5,551,740	Mean Sq = 173,492	

As shown in Figure 6, the treatment combinations with the larger means also tend to have a larger variance which suggests a possible need for transforming the data before analysis. However, examining the residual plot in Figure 8 indicates that the model used was adequate. The residuals, after fitting a linear model, give close agreement with the normal distribution, as shown in the normal probability plot. A substantial departure from linearity would indicate the possibility of invalid modeling assumptions. As an additional test of the model, a natural logarithm transformation of the data was performed. The results obtained after transformation, addressing the unequal variance, were virtually identical, thus confirming the original assumptions.

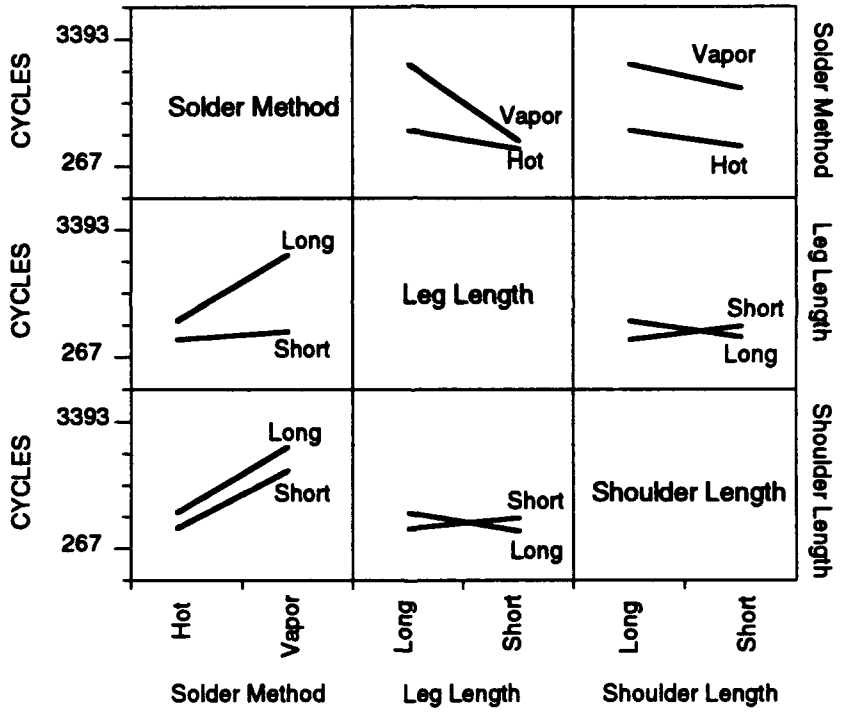


FIGURE 7. Two-way Interaction of Main Effects

Next, a Weibull distribution was fitted (via maximum likelihood) to the electrical failure data for each treatment combination. The Weibull is a two parameter distribution widely used to model fatigue and crack growth data [2]. The resulting parameter estimates were then used to estimate median lifetime, with 95% confidence limits as shown in Table 6. The results are also

presented in Figure 9, ordered by estimated median lifetime. These results are in general agreement with the analysis of variance results in Figure 6. There will be differences since the ANOVA simultaneously uses all the data and fits a linear model to assess the treatment main effects and interactions, while the Weibull analysis examines each treatment combination with five observations separately. When each treatment combination is analyzed separately, the confidence bounds for median life will necessarily be wider.

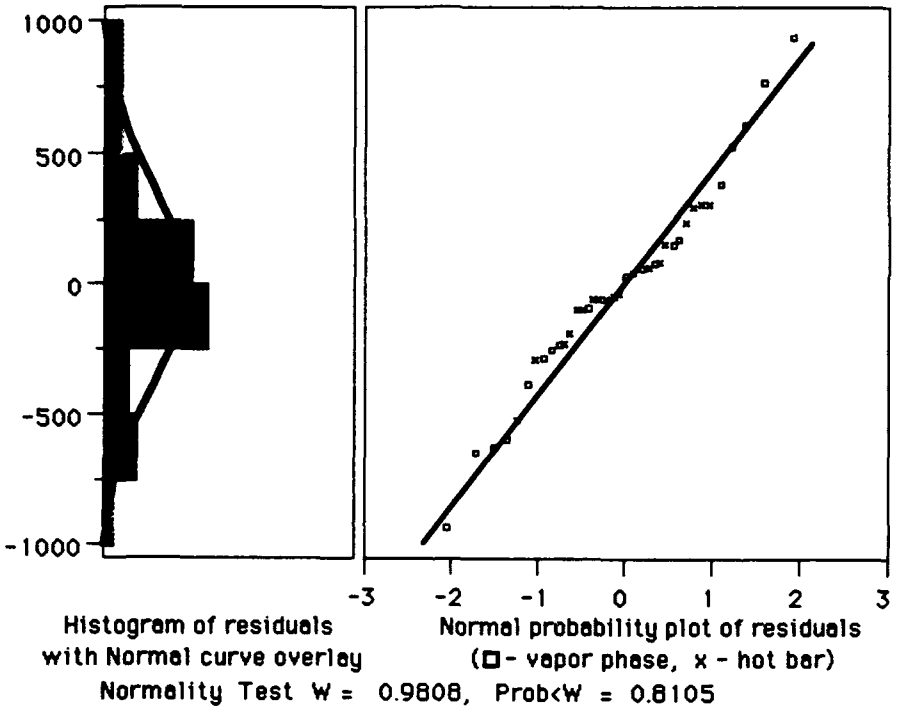


FIGURE 8. Residual Plot for Assessing Model

In summary, several basic conclusions can be made from the statistical analysis of the electrical failures. The solder technique had the largest impact on the solder joint life, with the high volume vapor phase joints performing significantly better (approximately 900 cycles longer life). The leg length was significant with long legs providing about 700 cycles longer life than short legs. In contrast, the shoulder length was not significant. The interaction between leg length and solder method caused the vapor phase/long leg combination to have a 300 cycle longer life than would be predicted by main effects only.

TABLE 6. Predicted Median Lifetime
with Approximate 95% Weibull Confidence Limits
(Number of Cycles to First Electrical Failure)

Treatment	Predicted Life	Lower Bound	Upper Bound
VLL	2809	2447	3225
VLS	2178	1587	2988
VSL	931	804	1077
VSS	1484	1146	1921
HLL	1148	984	1339
HLS	772	541	1100
HSL	722	614	849
HSS	1012	869	1178

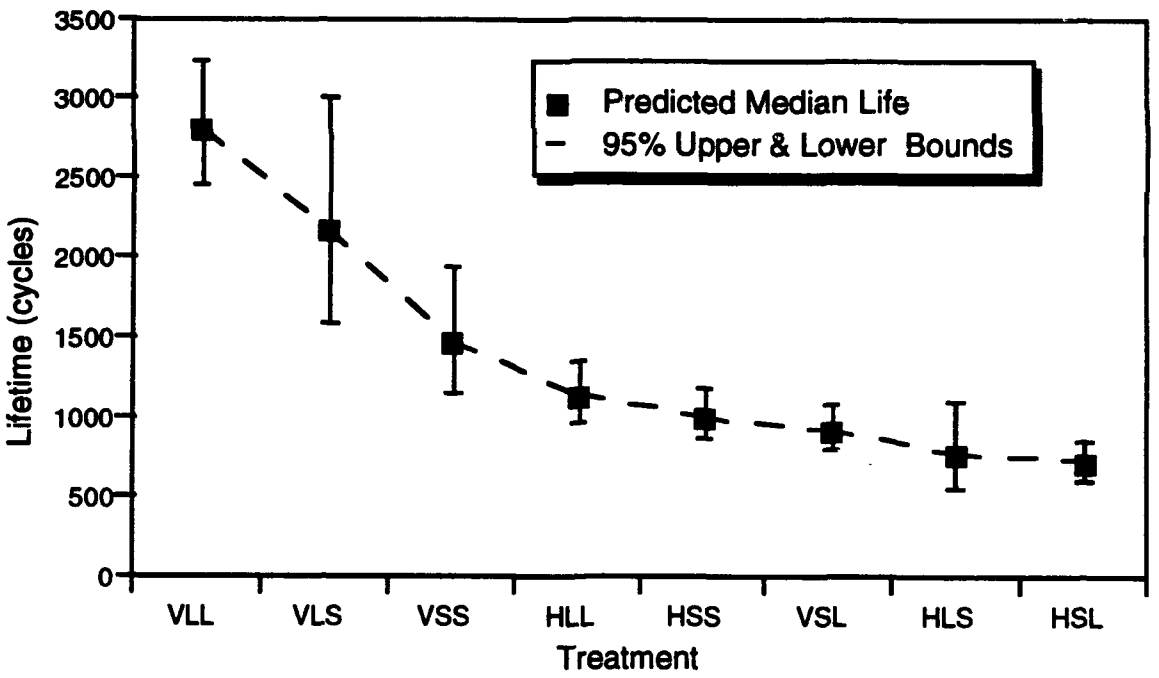


FIGURE 9. Predicted Median Lifetime
with Approximate 95% Weibull Confidence Limits
(Number of Cycles to First Electrical Failure)

Visual Crack Data

At irregular intervals during thermal shock testing, visual observations of cracks in the solder joints were recorded. Cracks were classified by a *crack score*, which indicates the length of the crack (see Table 3). A crack score of 0 designates no crack; a crack score of 3 indicates cracks longer than 50% of the foot length.

Due to the nature of the visual crack observation data, the analysis required some special handling. The number of cycles at crack initiation, where crack score equals 1, was available only in the form of an interval (n_1,n_2); after n_1 cycles, the crack score = 0, while by n_2 cycles, the crack score, X, was greater than zero. If X = 2, then the midpoint of the interval was used as crack initiation; if X = 3, indicating a longer crack, then 1/4 of the interval past n_1 was used; if X = 1, then 3/4 was used. This algorithm corresponds to more severe cracks most likely having initiated near the start of the interval, less severe near the end. Other methods of assigning crack initiation were tried, providing essentially the same results. For each treatment combination, median cycle time until crack initiation was estimated by fitting a Weibull distribution to the data as shown in Table 7. The median time until crack initiation, shown in Figure 10, generally followed the same treatment ordering as median time until electrical failure (Figure 9).

TABLE 7. Predicted Median Cycles until Visible Cracks in Corner Joints (with approximate 95% Weibull confidence limits)

Treatment	Predicted Life	Lower Bound	Upper Bound
VLL	997	924	1076
VLS	787	651	952
VSL	632	459	871
VSS	710	527	957
HLL	614	451	837
HLS	233	129	418
HSL	353	240	519
HSS	261	162	420

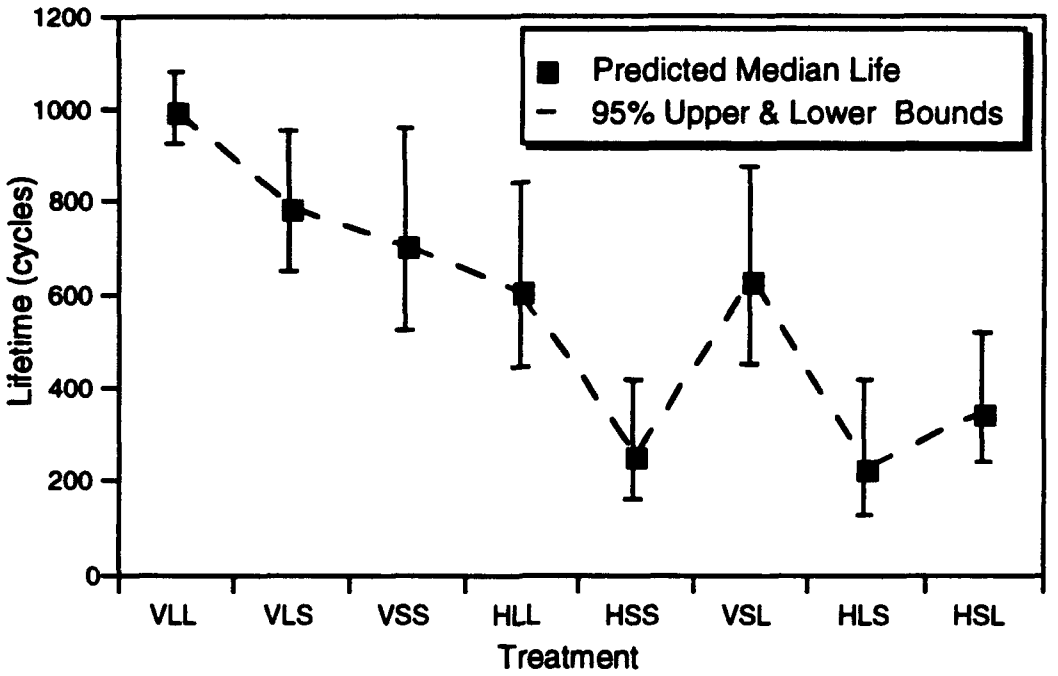


FIGURE 10. Predicted Median Cycles until Visible Cracks in Corner Joints (with approximate 95% Weibull confidence limits)

Several major observations can be made based on the analysis of this visual crack data. Cracks in the vapor phase samples grew more slowly than those in the hot bar soldered leads as shown in Figure 11 where the vapor phase lines lie below the hot bar lines, indicating less crack growth. The corner leads performed significantly worse with respect to crack growth (Figure 12), as indicated by all the values above the zero line; the corner leads had greater crack growth, and thus their average crack score was greater than the middle leads. This is in agreement with the theory that crack growth is faster where there is greater stress due to thermal mismatch.

The variability in crack growth between leads on the same side was significantly less than between leads from different sides. That is, although, at an inspection cycle, the leads may all have crack scores of 1's and 2's, they were not randomly distributed. For example, three sides may have all 1's and one side 1's and 2's or all 2's as shown in Figure 13. This phenomenon was observed across all treatments. This may be due to the part placement process, or simply due to the inspection process, and merits further investigation.

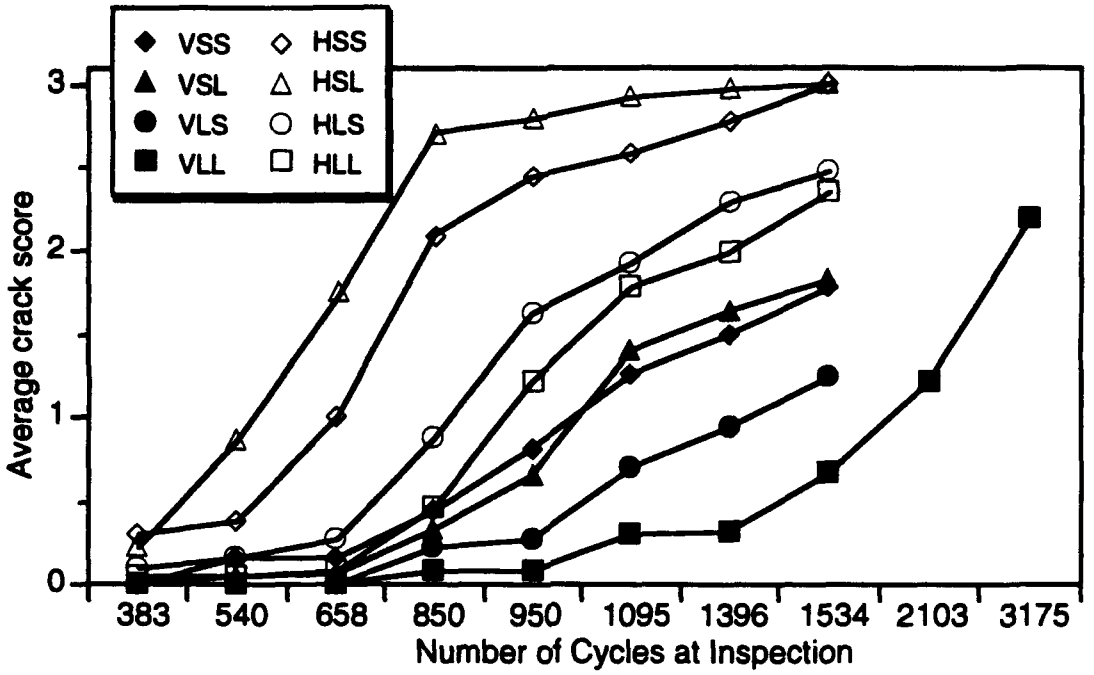


FIGURE 11. Average Crack Score by Cycles for Each Treatment
Caution: Arbitrary Non-linear Scale

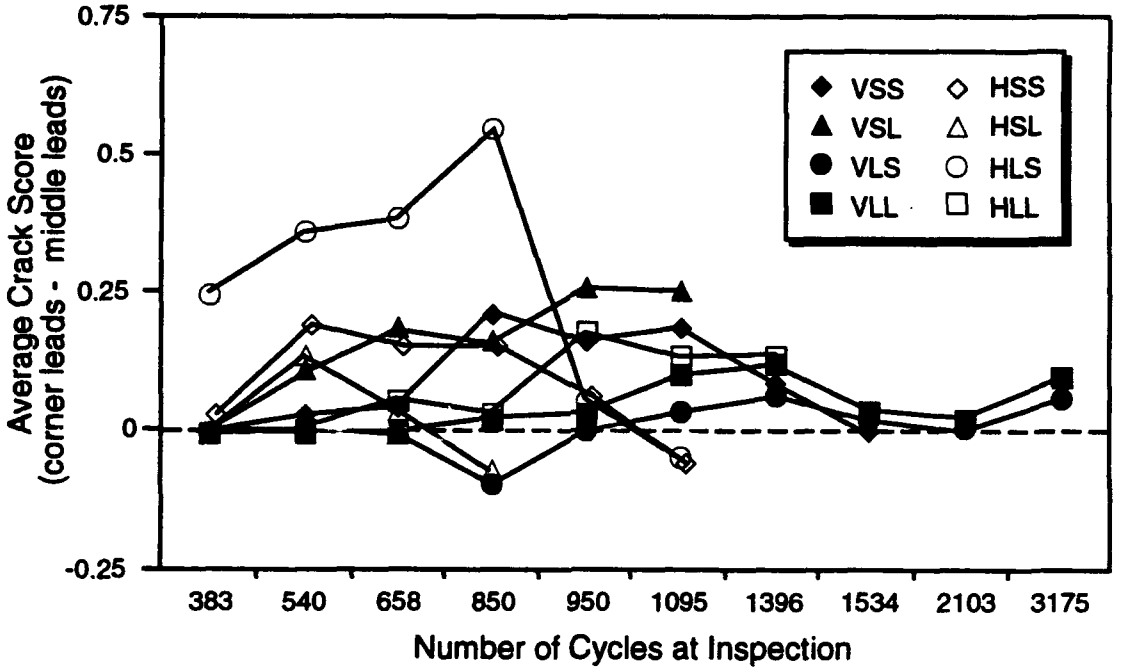


FIGURE 12. Average Crack Score (corner leads - middle leads) by Treatment
Caution: Arbitrary Non-linear Scale

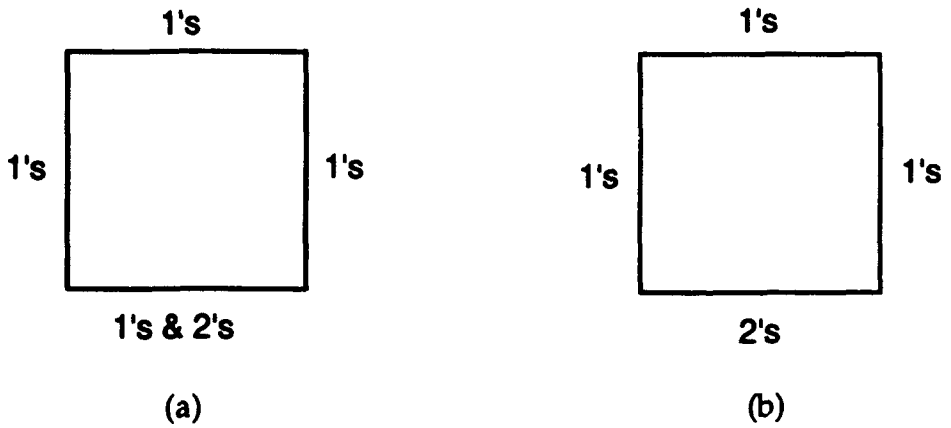


FIGURE 13. Typical Crack Score Patterns Observed

a. No variation on three sides, some variation on fourth side.
b. No variation on any of the four sides, but variation between sides.

FINITE ELEMENT ANALYSIS

Three-dimensional finite element models (FEMs) were constructed for two of the cases studied in this experiment. Figure 14 shows the long leg-long shoulder-low volume case representing the hot bar soldering method, and Figure 15 shows the corresponding high volume case representing the vapor phase soldering method. The Lawrence Livermore National Laboratory (LLNL) implicit finite element code known as Nike3d was used to perform the detailed nonlinear analysis. The analyses provide elastic and plastic strain responses as a function of temperature through the use of thermo-elastic-plastic constitutive equations for the solder material. Stress-strain curves [3] for 63/37 SnPb solder with a strain rate of 0.002/sec were incorporated in the analysis. For the transition rates between hot and cold used in this experiment, this strain rate was the most appropriate.

Features of the solder joints such as the thin solder regions and the shapes of the fillets required special attention to accommodate interfaces between sections with unequal meshes. The interfaces are referred to as "slidelines" and occur between the lead and the package, between the lead and the solder, and so forth. This capability is available in INGRID, the three-dimensional solid model preprocessor used with Nike3d. Special care was also taken to avoid pointed tetrahedral elements by using a small finite thickness along both sides of the solder fillets.

The FEM for the nonlinear analysis of the assembly includes the ceramic package, the Alloy 42 gull wing lead, the solder joint, the copper pad, and the substrate. An axially symmetric quarter section of the sample was modeled, and the corner lead was selected since it provided the maximum global coefficient of thermal expansion (CTE) mismatch. Including the substrate and the package served to define the load path. At the same time, the properties of the solder were allowed to vary as a function of temperature. Since the elevated temperature portion of the thermal cycle is the most significant factor in the heterogeneous coarsening of the solder microstructure and thus the failure of the solder joints [4], the assembly was subjected to incremental increases in temperature from 20 to 120 C. The total time used to cover the 100 C temperature increase was 100 seconds for both cases.

The effective plastic strain contours for the low volume case are shown in Figure 16. The maximum strain of 2.31×10^{-2} is found in the toe region of the joint. Figure 17 shows the contours of effective plastic strain for the high solder volume case. Note that the response indicates asymmetric loading. The maximum plastic strain of 2.08×10^{-2} occurs at the upper corner of the side fillet near the heel.The contours of effective stress in the leads for both cases are shown in Figures 18 and 19.

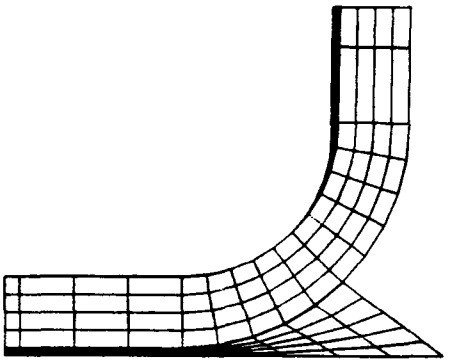


FIGURE 14. Finite Element Model (Low Volume)

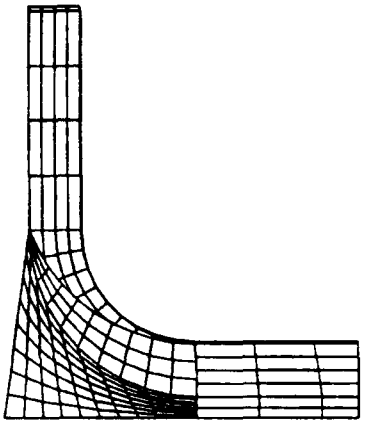


FIGURE 15. Finite Element Model (High Volume)

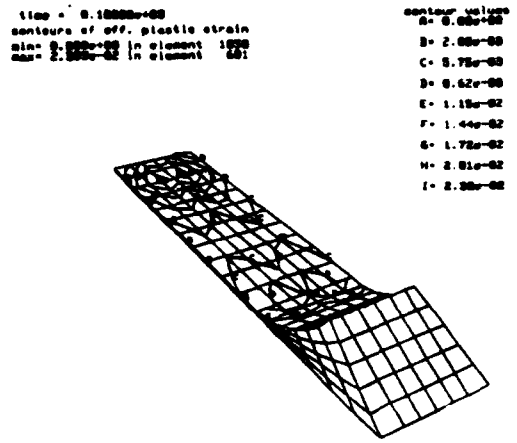


FIGURE 16. Effective Plastic Strain Contours (Low Volume)

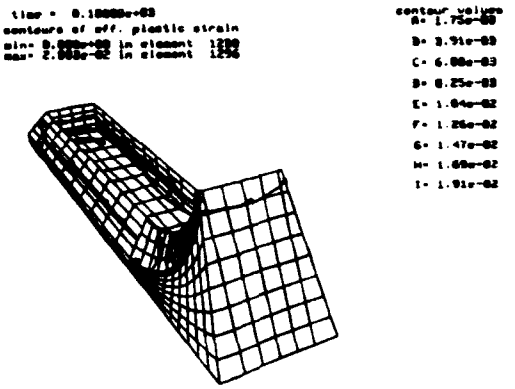


FIGURE 17. Effective Plastic Strain Contours (High Volume)

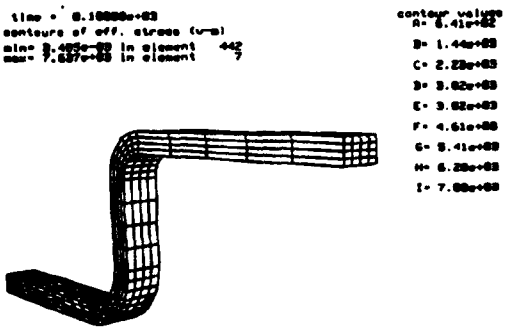


FIGURE 18. Effective Stress Contours in Lead (Low Volume)

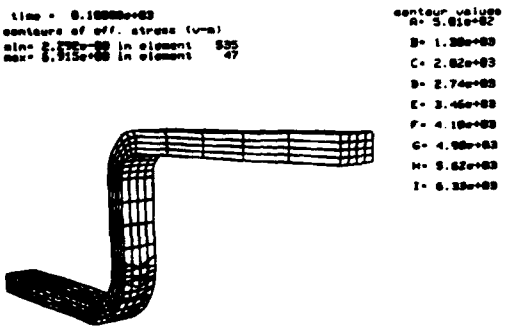


FIGURE 19. Effective Stress Contours in Lead (High Volume)

PREDICTION OF SOLDER JOINT FATIGUE LIFE

The effective plastic strain results from the finite element analysis can now be used to predict the solder joint fatigue life. However, it is necessary to first identify the failure mechanism(s) which predominate under a given set of conditions. D. Frear et. al. [4] have found from similarities between the full thermal cycle and the high temperature portion of the cycle that grain coarsening and cracking are dependent on strain at elevated temperatures. Thus, the Coffin-Manson relationship [5], which is a strain-based failure

criterion , was considered the most appropriate for this study. It relates the plastic shear strain range, $\Delta\gamma_p$, in the solder joint to the fatigue life as follows:

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma_p}{2\varepsilon_f}\right]^{\frac{1}{c}}$$

where N_f is the mean number of cycles to failure and ε_f and c are fatigue ductility parameters. For eutectic SnPb solder between -20 and 150 C, the values of these parameters are [6] :

$$\varepsilon_f = 0.325$$

$$c = -0.442 - 6x10^{-4}\overline{T}_S + 1.74x10^{-2}\ln\left(1+\frac{360}{T_D}\right)$$

Here $\overline{T}_S$ is the mean cycling temperature (in degrees C). T_D is the cyclic dwell time (in minutes). For this test, a nominal dwell time of 30 minutes was used. The value of the exponent, 1/c, is computed to be -2.39. Thus, any differences in plastic strain are amplified considerably.

Figure 20 shows the effective stress as a function of temperature for the low volume case. The initial time, t = 0, corresponds to room temperature, 20 C, and the termination time, t = 100 sec, corresponds to 120 C. Figure 21 shows the effective plastic strain behavior as a function of temperature for a group of elements in the failure region of the low volume solder joint. Notice that plasticity in the low volume case shows up at ΔT = 35 C. For the high volume case, Figures 22 and 23 show the effective stress and effective plastic strain, respectively, for two groups of elements, one group in the failure region and one group on the opposite side of the lead. The significant difference in plastic strain levels in Figure 23 reflects the asymmetrical nature of the load condition due to the corner position of the lead. In contrast to the low volume case, plasticity here appears at ΔT = 1 C, i.e. just one degree above room temperature.

The effective plastic strain results for both the high and low volume cases were used in the Coffin-Manson relationship to predict the number of cycles to failure. In the low volume case, the mean number of cycles until the corner joint fails is predicted to be 1450 cycles and in the high volume case, 1870 cycles. These analytical predictions can be compared with the experimental results for the number of cycles to failure:

	Low Volume	High Volume
Analytical Prediction	1450	1870
Experimental	1150	2810

Reasonable agreement is obtained for both cases with the predicted values being within roughly 30% of the experimental values.

It should be noted that this analysis does not account for solder creep, and thus a more complete, but more expensive, analysis using energy-based methods [7, 8] could also be performed to achieve more accuracy.

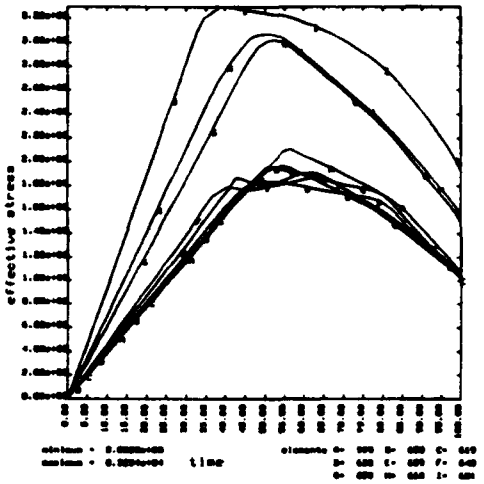


FIGURE 20. Low Volume - Effective Stress vs. ΔT

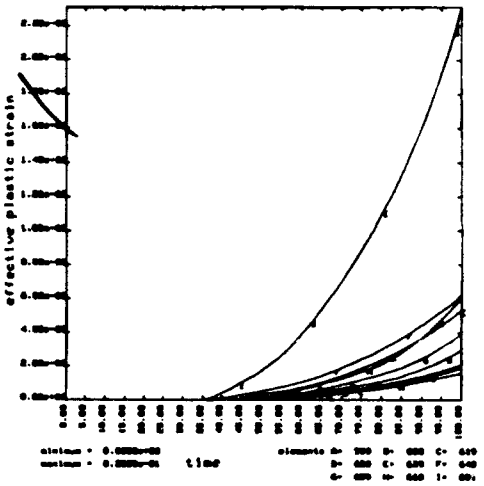


FIGURE 21. Low Volume - Effective Plastic Strain vs. ΔT

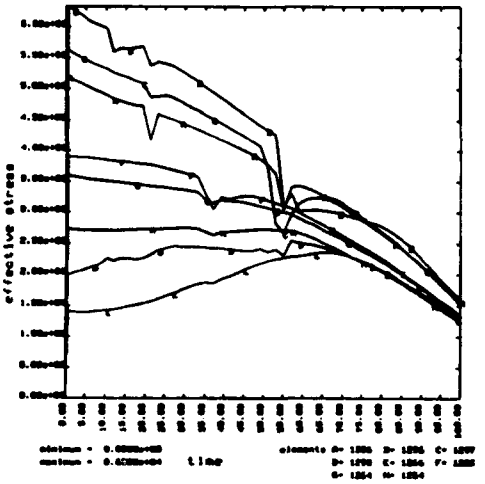


FIGURE 22. High Volume - Effective Stress vs. ΔT

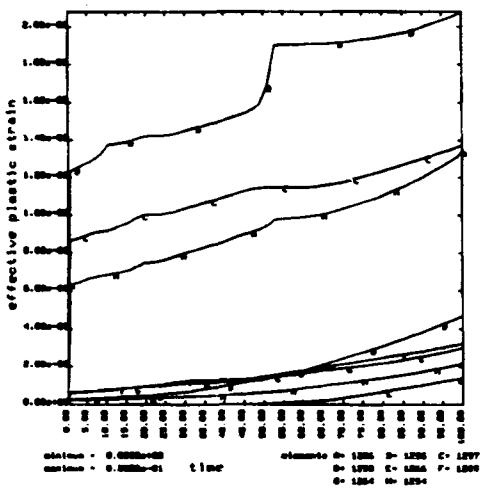


FIGURE 23. High Volume - Effective Plastic Strain vs. ΔT

DISCUSSION

Comparison Of Soldering Methods

Although solder volume was the primary distinguishing characteristic between the two soldering processes used in this experiment, it should be noted that there is another fundamental difference between the two methods. Vapor phase soldering is a non contact method and hot bar soldering is a contact method. It is known that this basic difference can lead to different failure mechanisms. For instance, whenever leads that are sufficiently non coplanar are soldered with a contact method which presses the leads down, the resulting residual stress in the joints can lead to early creep rupture failures [9]. However, based on the data in this particular experiment, no conclusions can be drawn about the comparative reliability of a vapor phase solder joint and a hot bar solder joint *when they have the same volume*. It is suspected that with good coplanarity and identical volumes, vapor phase soldering and hot bar soldering would provide similar reliability; however, in productior situations these prerequisites could be difficult to achieve consistently.

Use Of Closed Form Equations

Due to the ease of their use, the closed form equations introduced by Engelmaier [6] to predict the fatigue life of surface mount solder attachments have been widely applied to inappropriate situations, for example, to accelerated test environments such as the thermal shock test used in this experiment. Engelmaier admonishes against such misapplication of these equations [10] which tend to under predict, often severely, fatigue lives when incomplete stress relaxation occurs, as illustrated in Table 8.

It can easily be seen that when trying to determine solder fatigue lives, there are trade-offs in terms of cost, time, and effort versus accuracy attained. As mentioned earlier, even the FEA used here did not account for solder creep and stress relaxation, and various refinements could be made or other energy-based methods could be applied to achieve better accuracy.

TABLE 8. Comparison of Fatigue Life Estimation Methods

		Number of Cycles to Failure		
		Experiment	FEA[a]	Engelmaier[b]
High Volume	LL	2810	1870	380
	LS	2180		150
	SL	930		70
	SS	1480		30
Low Volume	LL	1150	1450	14
	LS	770		5
	SL	720		2
	SS	1010		1
Cost/Effort		Med-to-High	Med-to-High	Low
Time		High	Med-to-Low	Low

a: Finite Element Analysis with modified Coffin-Manson equation
b: Engelmaier closed form equation

Crack Growth During Fatigue Life

Since both the electrical failure data (corresponding to complete crack) and the visual crack observations are available (Tables 6, 7), they can be combined to obtain an estimate of the fraction of the solder joint life in which crack growth occurs. If N_f is the number of cycles until a complete crack exists and N_s is the number of cycles until the crack initiation, the fraction of the fatigue life in which crack growth occurs is:

$$\frac{N_f - N_s}{N_f}$$

The average value of this fraction is found to be 0.57 for the 0.050" pitch gull wing solder joints studied here. A similar analysis [11] was performed for thin small outline package (TSOP) solder joints, which are fine pitch and thus have a smaller solder joint length. For the TSOP, the fraction of the fatigue life during which crack growth occurs was found to be 0.25.

CONCLUSIONS

The experimental cases studied here provided a valuable set of solder joint reliability information including how the thermal fatigue life is affected by changing the gull wing lead bend configurations and by changing the soldering process. The statistical analysis of the electrical failures showed that the soldering method had the largest impact on the solder joint life with the high volume vapor phase joints performing significantly better than the lower volume hot bar soldered joints (averaging approximately 900 cycles longer life). Furthermore, the leg length was also significant with long legs providing about 700 cycles longer life than short legs. In contrast, the shoulder length was not significant which is a beneficial result for today's designs where PWB real estate is at a premium.

The visual crack data agreed with the electrical failure data in that the relative performance of the different cases was generally the same. Also, the visual crack data could be combined with the electrical failure data (corresponding to a complete crack) to obtain an estimate of the fraction of the solder joint life in which crack growth takes place. The average fraction of the fatigue life in which crack growth occurs was found to be 0.57 for the gull wing solder joint cases studied here.

Finally, the experimental cases studied here provided a wide variety of thermal fatigue lives which have been used to begin validation of a finite element analysis and subsequent prediction of fatigue life. The analytical results agreed reasonably well for both cases studied. Although more sophisticated analyses could be performed, the degree of agreement achieved here provides a high level of confidence, at an intermediate cost and effort expenditure, that this analytical approach could be extended to other cases. Use of this analytical approach, in combination with occasional verification experiments, provides a powerful tool in evaluation of electronics hardware design options for high reliability applications.

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Sandra Appl is a Materials Engineer with the Electronic Materials and Processes organization of Boeing Defense and Space Group. She has been with The Boeing Company for 8 years, working primarily in the areas of electronics assembly process development, materials evaluation, and solder joint reliability.

Sandra received a B.A. degree in Physics from the University of Kansas, attended the Swiss Federal Institute of Technology in Zurich, Switzerland as a graduate exchange fellow, and received an M.S. degree in Solid State Physics from Iowa State University. She is a member of ASM International.

Address: Boeing Defense and Space Group
P. O. Box 3999, MS 9E-97
Seattle, WA 98124-2499

Karen Coates is an Electronic Materials and Processes Engineer at Boeing Defense and Space Group. Her major responsibilities have included various surface mount process development and reliability studies.

Karen has a B.S. degree in Ceramic Engineering from the University of Washington and an M.S degree in Materials Science and Engineering from Stanford University. In addition, she has over 7 years of experience in electronic materials processing, including silicon wafer cleaning, tape automated bonding, and advanced assembly.

Address: Boeing Defense and Space Group
P. O. Box 3999, MS 9E-97
Seattle, WA 98124-2499

Mostafa Rassaian is a Structural Dynamics Engineer with the Advanced Packaging organization of Boeing Defense and Space Group. He has developed computational methods for avionics integrity assessments using structural and fatigue concepts and has applied nonlinear finite element methods to various surface mount technology designs, as well as to address hermeticity in fiber optics.

Mostafa received his Ph.D. in Applied Mechanics from the Illinois Institute of Technology in Chicago. He is the author of numerous works dealing with applied mechanics problems, with an emphasis on nonlinear finite element methods.

Address: Boeing Defense and Space Group
P. O. Box 3999, MS 9F-15
Seattle, WA 98124-2499

David Rose is an applied statistician with the Mathematics and Engineering Analysis organization of Boeing Computer Services. He has focused attention on the design and analysis of experiments in the engineering and manufacturing areas of Boeing. He has also been involved in reliability and life testing and teaching statistical procedures to the engineering community.

David received his B.A. degree in Mathematics from Washington State University and his Ph.D. in Biostatistics from the University of Washington. He is the author of numerous papers and technical reports on statistical theory and its application.

Address: Boeing Computer Services
P. O. Box 24346, MS 7L-22
Seattle, WA 98124-0346

SMT CONSIDERATIONS IN SPACEFLIGHT AND CRITICAL MILITARY APPLICATIONS

by

George S. F. Orsten, Senior Staff Scientist, RDD;
William New, Technical Consultant, SSD;
Yun Wang, Mechanical Engineer, SSD;
Marc L. Peloquin, Senior Design Engineer, RDD;
Lockheed Missiles and Space Company
Sunnyvale, CA.

ABSTRACT

Lockheed Missiles and Space Corporation has three separate SMT lines currently operating in two different locations in the San Jose bay area. One of these lines, operating at one location, was NASA certified for spaceflight work by NASA-GODDARD in January of 1991. The other lines are currently being certified to MIL-STD-2000A. Data has been taken over the last three years on thousands of solder joints, for gullwing, J-lead, and leadless components, varying in size from 0405 chip resistors to fine pitch components almost 2" on a side. This data comes partly from the certification process for the lines, but mostly from research on reliability under company funded programs.

Some of the data was taken using more than 1000 thermal cycles with no interruption, and final analysis and examination only after total test completion. Some of the data was also taken on more than 1000 cycles, but examining the boards every 50 cycles. During these tests, a certain number of joints were sacrificed for complete testing of grain size, and all joints were examined to see if the initiation of microcracks could be seen. Reworked joints were also tested, to see if there were any differences between them and joints made at the initial build.

Data was taken on solder joints made with alignment good enough that there was no overhang of the device leads over the pads on the board. A second run was made with overhang almost exactly equalling the 25% allowed in MIL-STD-2000A.

The paper presents not only some test results, but the development of certain philosophies for design and construction that resulted from the data.

INTRODUCTION

In 1989, two of the authors (Orsten, Peloquin) were tasked with building two satellite power systems, at the Palo Alto Research Labs of Lockheed. The space and weight requirements were such that SMT was mandatory, and an SMT facility was developed with the view of having it approved by NASA-GODDARD for space hardware. The final audit took place on 15, 16 and 17 Jan 1991, at which point temporary approval was granted, pending the completion of 1000 cycles of thermal testing of the qualification boards which had been built during the audit. The units passed the test which was completed in April of that year, and the final approval was issued in May 1991. Orsten also wrote a complete specification document, as there was no NASA specification covering SMT at that time. This document required, among other things, that every SMT component that would be on a board would first be tested to the equations developed by Engelmaier et al, using the mission environment data as well as the data for the P.C. board and the component in question. To make this economically feasible, we developed software in the form of spreadsheets for every class of components, so that the test of a single unit took less than 1 minute. The major effort here was for leaded components; the stiffness parameter Kd needs to be calculated, and there are about 6 variables in this alone. For people designing for aerospace in particular, but in reality, any high reliability system, such software must be available. We now have sets for flatpacks in gullwing configuration, quad flatpacks, J-leads, chip components, and round leaded devices. We test any proposed system before board design is even started.

In the meantime, the Space Systems Division of the company, operating in Sunnyvale, was bringing an SMT line up, intended for space hardware. This work was done by a larger team, headed up primarily by the other two authors of this paper, (New, Wang). This team also did a lot of assembly and thermal cycling tests, but as they were not reporting to any particular agency at the time, they had freedom to do their testing somewhat differently. They had much larger quantities of boards and solder joints, and they examined these after every 50 cycles, including a few sacrificial tests each time, to check on grain size and other metallurgical characteristics.

To integrate the work of both divisions, Orsten and Peloquin temporarily moved to the SSD facility in August of 1992. Test data was combined, and many things were discovered that the separate organizations might not have found out so quickly.

THERMAL EXPANSION STRESS PROBLEMS

The first thing that came out of the tests was that you MUST test the Tce for any board you are proposing to use with a high number of thermal cycles. Typically in space at Low Earth Orbits, (LEO), you see 29200 cycles in 5 years, and about 47000 cycles in 7 years. Neither of these numbers is particularly unusual in this business. We noticed on

both sets of tests that we were getting no failures at all, well past the time we expected; we had used "textbook" values for Tce for the polyimide boards we were using. We finally measured the actual Tce or our test board, which like most such test boards was a single sided board, no ground planes, no prepreg layers, etc. Instead of the 14 ppm value that we had anticipated, we were at approximately 11! The ΔTce between the chip and the substrate therefore was 5 instead of the 8 we thought we had. The lesson here is that very simple one or two sided boards commonly used for thermal cycling tests have Tce values far lower than we commonly think of for that material.

Measuring the actual value is easily done, as long as you avoid complex measurement techniques and get back to fundamentals! Make a jig similar to the one in Figure 1.

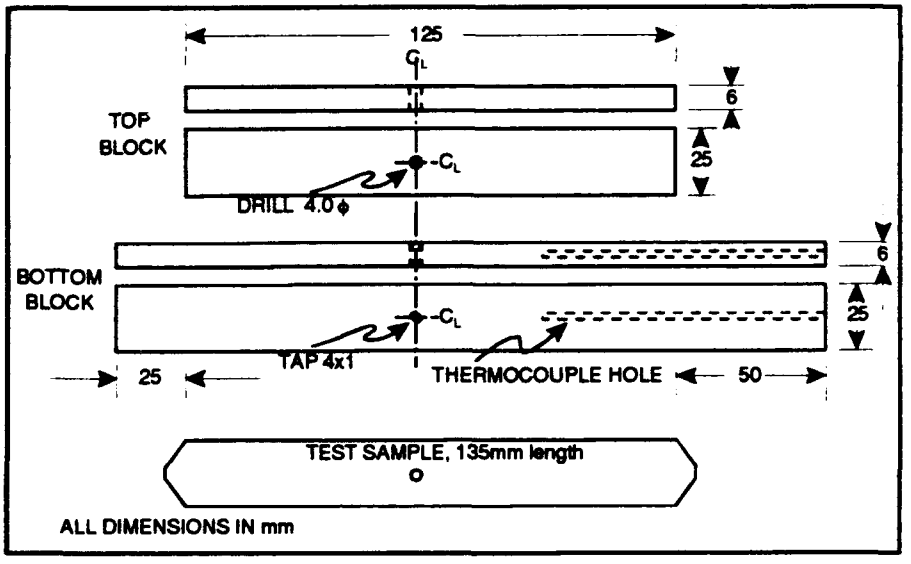

FIGURE 1. Measurement jig for Tce of P.C. boards

It is a block of aluminum that clamps the sample which is about 2cm wide, and about 14 cm long. A hole in the bottom block allows you to "bury" a thermocouple in the middle of the block. The ends of the test sample can be reached directly using an electronic dial caliper; We use a Starret model that costs about $200, and gives measures to 0.001 mm on the metric scale, or its U.S. equivalent. Note that most electronic 6" calipers do not give a full 10 digits in the last place, they only give you a "0" or "5". The model we use also prints out directly with a small cable, or can load to a P.C. computer.

Put the jig with the board sample clamped in the middle in a temperature chamber and heat or cool it, letting it stabilize at the required temperature. Open the door and make three quick measurements; you can then average if you like, before the temperature changes more than 1°C. The lower plate of the jig is larger, so you can rest the jaws of the calipers on them, for ease of measurement.

To make things a bit less hectic, we recommend that you have a teflon block with a cavity milled in it, sitting in the oven, next to the jig. As soon as the oven door is opened, place the jig into the block to slow down heat transfer to the outside. Another smaller cover over the top helps also. It allows time to make several measurements without haste. The shape of the test sample is important on the ends, the drawing shows the recommended shape, so that caliper position does not become too critical.

An example of such a test run is shown here in its original form. It is a 17 layer polyimide board, 0.125" thick!

****

Test Item Part Number: 8541774-001 REV-A SN: 884 DC: 9228

OVERALL CALCULATIONS OF Tce

RAW DATA:		CALCULATED RESULTS	
Temp, (T) °C	length,(l), mm.	Tce to -42	Tce to +123
-42	143.06	-	18.19
-15	143.14	20.71	17.70
+21	143.24	19.96	17.10
+73	143.37	18.82	16.73
+123	143.49	18.19	-

CALCULATIONS BETWEEN ADJACENT TEMPERATURE POINTS

Temp, (T) °C	ΔT	Δl	Tce,(ppm/°C)
-42			
	27	0.08	20.71
-15			
	36	0.10	19.40
+21			
	52	0.13	17.44
+73			
	50	0.12	16.73
+123			

Note: $Tce=\Delta l_{(mm)} x 1{,}000{,}000/(l_{mean} x \Delta T_{(°C)})$

****

The overall Tce is 18.19ppm/°C, a value not unexpected for a 17 layer board. Note that the Tce value increases steadily with decreasing temperature. This is significant, since many satellite applications tend to run on the cold side.

Once the real Tce is established, the calculations for end life can be done, but note that you need to know the mean temperature for the mission environment, not just the ΔT! That establishes the value for your substrate Tce that will be used in the calculations.

By now, everyone should be familiar with Englemaier's equations, (Reference 1). We present them, once more:

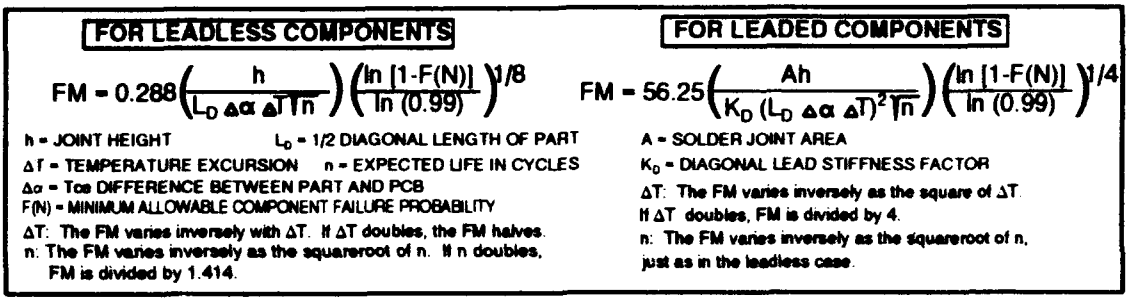

FIGURE 2. The Engelmaier life prediction equations

It is rather obvious that one can also solve for "n", the number of cycles, by setting Fm=1, and algebraic transposition. In that case, the equations look like this:

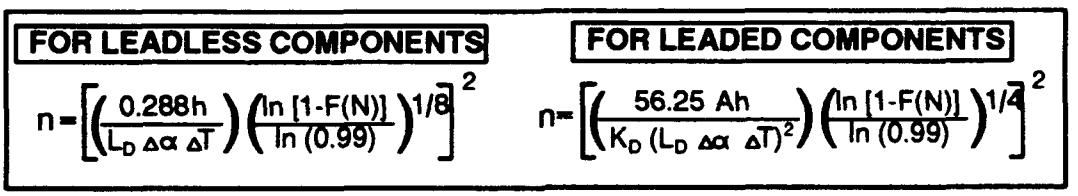

FIGURE 3. The Engelmaier equations rearranged for "n".

Spreadsheet calculations can be set up for either case. The major complication is the calculation for Kd for the leaded case. There are several methods suggested for this, one of the most complete being the work of Robert W. Kotlowitz, (Reference 2). Coding this in is a major effort, and will require major amounts of time for accuracy checking. Simpler methods than those of Kotlowitz are available, and the common cantilever method of any textbook such as Eshbach's Engineering Fundamentals Handbook will work, but at slightly degraded accuracy. Figures 4 and 5 show some of the spreadsheets that were set up, solving for Fm. They now exist for leadless parts of all types, MIL flatpacks in gullwing configuration, quad flatpacks formed the same way, and J-leaded packages. We add to these as we need them.

The Figure 4 spreadsheet shows a common 16 lead Mil Flatpack, formed in gullwing configuration. Note that it passes 10,000 cycles, with a ΔT of 30°C, when there is a mismatch of 7ppm. The figure of merit Fm is 1.49, so there is even some margin. The spreadsheet printout has been altered a little for publication. The grey areas are protected cells, while in the real screen presentation, they are colored yellow instead. This means that the engineer entering data can not accidentally erase or alter any of the equations or constants. The storage are for Tce and Young modulus values also shows, as do some intermediate calculations that are handy to have. If an "ERROR" signal comes up on the

right hand side under the "Leads" or "Case" column, it means that you have either entered two "1"s or two "0"s where you had to choose between copper or kovar for leads, and ceramic or brass for the case. It has to be one or the other, it can't be both! The brass value is also not too far away from plastic parts, but the engineer can unprotect a given cell and change a constant value for a given calculation, as long as the results are not "saved".

INPUT DATA FOR CHIP	PARAMETERS		
n=number of leads per side	8		
g=pitch of leads	.050		
b=width of lead	25		
t=lead thickness	.007		
s=straight portion of lead	.040		
d=length of leg	.070	Tee	YOUNG'S
l=length of pad contact	.060	STORAGE	MODULUS
Φ=Angle of bend	90		STORAGE
L=length of body	.250		
Lead is Copper - enter 1, else 0	1	17.70	1.6e7
Lead is Kovar - enter 1, else 0	0	5.00	3e7
Case is ceramic - enter 1, else 0	1	6.20	
Case is brass - enter 1, else 0	0	20.40	
OUTPUT DATA FOR CHIP	**ANSWERS:**	**Check on ERROR**	
Area of contact	.015	Leads	Case
Effective Tee for chip	8.398	1.00	1.00
Half diagonal length	.262		
Moment of inertia, lead	7.145833e-9		
Kd=stiffness factor	990.1		
CALCULATIONS OF BOARD PARAMETERS			
INPUT DATA FOR BOARD	**PARAMETERS**	**INTERMEDIATE CALCULATION**	
Tee for substrate, (ppm)	16	Δ Tee	7.812121e-6
number of cycles, life time	10000	SQRT of n	100.00
ΔT for each cycle, (°C)	30		
h=height, (usually 0.003)	.003	K(56.25)*A*h	2.53125e-3
F(N)=min. allow. failure rate	.00001	Prob. Mult.	.18
OUTPUT DATA, F_M, Figure of Merit	1.49		

FIGURE 4. Spreadsheet printout for the program called "FLATLEAD.CAL", which calculates the Figure of Merit, (F_M) for flatpack components.,

The Fig.5 printout shows a 1206 chip component. The spreadsheet is simpler, since the equations are simpler, and there is no lead data to enter, or stiffness factor, Kd, to calculate. But this particular spreadsheet is also for LCCCs, and so there is room to enter the pitch and the number of leads per side. When the leads per side is "1", then the pitch

parameter is not used, and the chip width is calculated to be the same as the castellation width. We see here a unit that does not meet specifications, the Fm value is 0.65.

CHIP DATA INPUT:			
Tce - Comp.	6.4 ppm		
Length	.12 in.		
Lead or Castellation Width	.06 in.		
Pitch	.05 in.		
Number Leads per Side	1		
Joint Height	.003 in.		
CHIP CALCULATIONS:			
Effective Chip Width	.06 in.		
Half Diagonal Length	.06708 in.		
MISSION DATA INPUTS:		**CALCULATIONS:**	
F (N) = min. allow. failure rate	.00001	Prob. Mult.	4.214e-1
Tce - Substr.	14 ppm.	Δ Tce	7.6e-6
cycles (n)	3000		
ΔT	20 °C.		
CHIP / MISSION RESULTS:			
FIG. OF MERIT	6.5e-1		

FIGURE 5. Spreadsheet printout of the "NOLEAD.CAL" program, which calculates the Figure of Merit, (F_M), for chip and LCCC parts.

All these spreadsheet models run on an IBM clone, 386-40, with 8 Mb of memory and a 387 coprocessor. The software is Supercalc 5.5, a program we like for technical use because of its transcendental function handling.

The other programs are "J-LEAD.CAL", "QUADLEAD.CAL" and "RNDLEAD.CAL". The names are self-explanatory, they were picked for ease in remembering what they were for. The roundlead program is abbreviated because of filelength limitations, it is used for axial leaded special components that are "converted" to SMT use. Usually, these are high voltage diodes and the like.

PLACEMENT REQUIREMENTS

MIL-STD-2000A allows 25% overhang for most parts placement. The specification we wrote for NASA allows no overhang at all, and the current specification we are using for the SSD SMT line echoes that philosophy. The reasons for that come from testing that was done in 1992 for over 1000 thermal cycles of -35°C to +125°C. About 7000 solder joints where the foot of the component was totally on the land were cycled for over 1000

cycles. There were no failures in any joints. A second batch was prepared, in which the automated placement equipment was programmed to offset the part by almost exactly 25%, to be just within the MIL-STD-2000A limit. These boards were then also cycled, to the same test specification. There were 2.02% failures at 400 cycles! Test were discontinued at that point to free up scarce test equipment resources for more useful purposes. Solder joints with 25% offset did not appear to us to be very useful.

Another item noted in these tests was that solder joints with ample toe fillets showed much less stress than those with minimal or no toe fillets. This is a subjective observation, but it agrees well with the data in "Surface Mount Technology" by Carmen Capillo, page 99, Fig. 6.19, where lifetime is shown as a function of land extension beyond the chip, with values between "0" and ".050". Between .005" and .050", lifetime for a 16 "pin" LCC goes from 200 to 600 thermal cycles over the full MIL range. The preceding page in this book also gives some data from the AMP Corporation, for leaded device considerations, and we will not repeat them here.

The combination of toe fillet requirements and land width sufficient to insure that the part can be placed totally on the lands requires that the CAD part libraries be examined with great care. Many commercial supplied libraries are not adequate for space applications. The high reliability user must be prepared to generate his own libraries, and enforce their use. At the RDD facility, we have completed the generation of a complete library, of several thousand parts. The problem is always one of translation, when a company uses at least 8 different CAD packages, on at least four different platforms! Generating these libraries is not a job for a draftsman. A good engineer, using all the data available as to both size, and, most important, tolerances, needs to create the exact patterns to make sure that they are adequate. Translation is sometimes possible "in the back door", by using Gerber files. Some programs can read them in, and of course, all programs will output them.

SOLDER, REWORK AND NITROGEN ENVIRONMENTS

The properties of eutectic versus non-eutectic solders is well enough known that it should not require much comment, but it is non-the-less instructive to study the phase diagram in Fig. 6, below.

The assembly is at risk the entire time that solder is in the paste state, for non-eutectic solders. While it is in the liquid state, and after it is in the solid state, no amount of vibration will give you a disturbed, or "cold" solder joint. Eutectic solder has no paste state, and moves directly from liquid to solid state, so the risk time is very short, basically the time difference between the hottest and coldest spot on the board. But for non-eutectic solder, it can be quite long. Assuming that you are cooling about 1°/second, you can be at risk for half a minute with Sn55. Now no one would knowingly use Sn55

solder paste, in fact as far as we know, you can't buy it! But you can make it yourself, quite unintentionally, out of your good Sn63! Both tin and lead oxidize, and NOT at the same rate. If you subject molten solder to an oxidizing atmosphere, the differential oxidation rate will create a new solder with a higher lead percentage. If you do it both at initial reflow, and then at rework as well, you can get to Sn55 quite easily. The nasty grey appearance of the joint is simply a joint that has the same slag as you see on the top of your solderpot, which you usually skim off, but now it is deposited all over the joint area. You also need more heat for rework, and this just burns up more tin! Both the P.C. board and the parts are now being subjected to unnecessary stress. The issue of the amount of intermetallic compounds that are formed with the copper also comes into question as the time and temperature both increase.

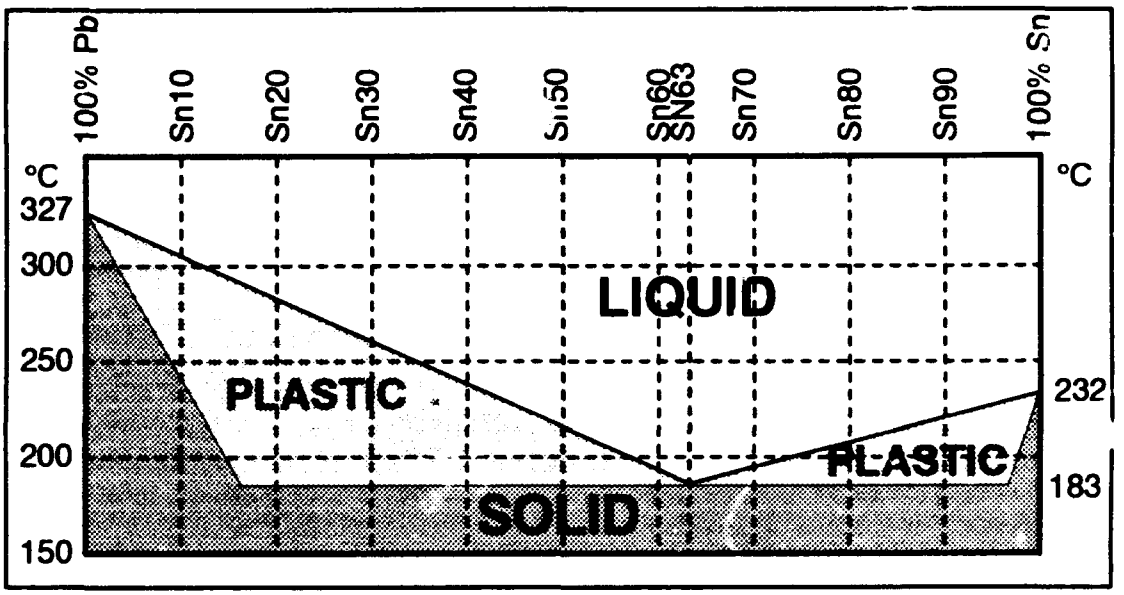

FIGURE 6. Phase diagram for Tin-Lead mixture solder

The answer to this problem is simple. You reflow in nitrogen or with a vapor phase system, but NEVER air. In addition, your hot gas type rework machines operate with nitrogen. If you don't know the history of a joint, or for safety, even if you do, and a part is being replaced, remove all the old solder by wicking or with a vacuum tool. Apply the correct amount of fresh Sn63 solder paste, and keep going. A reworked joint should be indistinguishable from the original well made joint, by any test you care to make. We use digitally controlled paste application tools, with charts to show the operator the exact settings and needle diameter for any land size, to apply the same amount of paste that the stencil would have done. Needless to say, the temperature of the paste must be reasonably controlled so that viscosity is known. Cold paste right out of refrigerated storage can't be used until it warms up. We found quite accidentally that machines that have hotplates for preheating the bottom gave us better results than those that use hot gas

jets from underneath, even though they are somewhat slower. This occurred when we bought a new machine that had a hotplate and tried it out. As a result, we converted all our rework stations to use such hotplates.

There is one further warning on rework. It is common in some places to rework small chip components such as a 1206 part with hot tweezers to remove the part, and then a soldering iron to resolder the new part. Anyone that has tried this knows that the operator has to hold down the new part, as it tries desperately to get away from the hot iron! Usually you "spear" it down with an orange stick. **And when you do this, the "h" parameter in the Englemaier equation goes from 0.003 to about 0.0002!** If you now try to fly this board, that part will come off about 8% into the mission life cycle! You can't rework like that. Again, hot nitrogen tools with very low velocities so that the part and the solder are not blown around are the answers.

All these rework tools operating with hot gas have to be characterized very carefully. We find that the vendor of the system often does not really know what the machine does, in terms of predicting the operating temperature at the board versus flow-rate settings, heat control settings, nozzle choices, and other machine variables. There is no way out of this other than to take your own data. Design of Experiment (DOE) techniques can minimize the amount of data you need to take to fully characterize your machine. A paper will shortly be submitted to Surface Mount Technology Magazine by Mr. Thomas Clifford of LMSC describing how to use DOE as a tool to set up these tests. When you are all done, you should be able to have a chart at the operator station, that gives every machine setting, including time, to do both the removal and re-application of any given type of component. Allowances must be made for unusual board types with great heat-sinking capabilities, but with a large area bottom hotplate, set at 125°C, and allowing the board to come up to that temperature, the ΔT between the board and the immediate rework area is only about 65°C, so the gradients are small.

ADHESIVES PROBLEMS

Adhesives will be the single largest problem in high reliability SMT production. It is a problem that if you are starting from the beginning, it may take you more than a year of constant research to solve. Adhesives are needed for two purposes. First of all, any part such as a gullwing will need to have some adhesive bonding or staking in order to survive vibration testing and the launch environment. Secondly, high power parts will require adhesives that have high thermal conductivity to conduct the heat to the board. In either case, for space applications, you need something that does not outgas, has the requisite thermal conductivity, is easily dispensed, and has a long pot life. If it requires thermal curing, and has been applied right after the solder stencil operation, it cannot take too long to cure, and must be cured in a inert atmosphere, since the whole time this is going on, the solder is still in paste form and can oxidize. Ideally reflow and thermal cure of the

adhesive can be done together. We have purchased a 24 zone convection reflow oven that holds <100ppm of O_2 so that we have sufficient time available to cure adhesives. In effect, we have lengthened the bakeout phase to insure cure.

In addition, the adhesive is not allowed to lift the component, either at cure as part of the cure process, nor at reflow as part of the normal thermal expansion process for a (now) completely cured adhesive. If it lifts the part up more than 1 mil, it will lift the feet of fine pitch parts right out of the solder paste. Almost all adhesives have this property, you will find very few that are usable. You must ensure that there is no air entrapment in the uncured substance, that the pattern put under a component is higher in the center, like a pyramid, and that you will cover a sufficient percentage of the area of the part to effect adequate heat removal. The pyramid shape ensures that there is no slump in the center that will entrap air as you place the part, and that air is forced out all along the perimeter of the part as it comes down. If you put too much adhesive down, it will squeeze out over the lands, and you have a problem there. Some companies inject the adhesive through a hole in the back of the board after assembly, but this limits the layout when you have components on both sides, which is the common thing today. Also, you become very unaware of thermal expansion this way since you do not immediately see the effect. Unfortunately, under thermal cycling, there is a tension force placed on all the leads, as the adhesive expands and tries to push the part off the board. The amount of the force has to be calculated, and this requires knowledge of the Young Modulus of the cured adhesive. You will need to take the data yourself, because virtually no manufacturer has any idea what it is for his product. This force then has to be added vectorially with the other forces to arrive at a lifetime prediction using the Englemaier relationships.

CLEANING AND CLEANLINESS

The requirements for cleaning space borne circuitry in particular are well known, but not always so well understood by the organizations doing the assembly. Most people think that leaving some flux residue will result in corrosion after some time, and therefore that is why you have to clean it. Considering that in the old days of vacuum tubes, we never cleaned the terminal boards that held all our resistors and capacitors at all, nor did we clean the tube sockets after soldering, you begin to wonder about this. Some of those circuits lasted well over 40 years! In use, it is unlikely that the joint will be reheated up to 170°C, which is the activation temperature for the flux, so what is the real problem? The answer is that the real problem is the same problem that causes us to have to check for outgassing or weight loss in vacuum of adhesives, and eliminates at least half the ones we would like to use! In vacuum, any residual flux will outgas, and as there is no gravity to cause the vapor to go to any particular place, it will hover around all the satellite, and deposit itself on everything; just like vapor deposition, for that is really what we are talking about! All your optics will now have a nice rosin coating, and the absorption

spectra that you get for data will cause numerous very interesting papers to be written in the physics journals of the world, theorizing why the universe is full of flux!

Cleaning behind the heel fillets of fine pitch parts that are mounted quite close to the board is not easy. Most of the cleaning machines we have tried could not do it, with any solvent we used. Only one machine has given us consistently good results, and then with only one solvent! Remember that we are automatically disregarding any solvents that violate the Montreal protocol. This is not an easy problem, we have bought and then discarded two fairly expensive cleaners without ever having brought them successfully up on the line.

Another allied problem showed up on a board that was being built on one of our lines. This concerned cleanliness during assembly. After reflow, Mr. Peloquin noticed that there appeared to something like a blowhole on the face of a fillet. With very high magnification, he discovered that a thread-like fiber had been caught between the land and the foot of the part, and buried in the solderpaste. What looked like a blowhole was actually a case of dewetting around the thread. When he continued looking at the joint, section by section, he discovered that the thread went all the way out the back of the joint, so there was a tiny hole all the way through. Elementary stress analysis will tell you that this is a place for stress buildup, and crack formation to start. Incidentally, this sort of thing would have never been seen at 10X or 15X, we were using 100X on that day, and our usual checks on the main robotic line are done at 48X which is as high as the variable control on the inspection machine goes.

As a result, we are very careful in the cleanliness of the operations, especially between the cleaning of the stencil, through paste application, and finally the pick and place operation. The NASA certified line operates totally in a clean room, under laminar flow benches that typically check out at less than 3 or 4 parts per cubic foot. The room is well within class 10,000, and usually measures somewhere between 1000 and 2000. Head and facial hair coverings are taken for granted. The robotics line is not in quite as clean an environment, but we are surrounding that area with laminar flow benches running 24 hours a day. This results in localized scrubbing of the air, and does a remarkable cleaning job. Extreme caution must be used with air hoses and vacuum cleaners. Our vacuum cleaners are models that have HEPA filters at the output, and are intended for clean room operation.

SUMMARY

It is not possible to put down in one paper of this size, all the special considerations that are needed for high reliability circuit assemblies, especially satellites in LEO applications. In general though, we can list some of the most significant ones: 1: Calculate all the lifetimes early in the design cycle, and do not get committed to a design

or a board material before knowing that it can survive the mission. 2: Know what the board characteristics are before your design is frozen, measure it. 3: Placement accuracy has to be much better than MIL-STD-2000A, and therefore, land patterns are more critical than they are for building C-D players! 4: Heating in an oxidizing atmosphere is not satisfactory, at either initial reflow or at rework. 5: Equipment such as rework machinery has to be carefully characterized for performance. The manufacturer usually doe not have the data to the degree of accuracy you want. When the sales rep of our equipment saw our own data, he really wanted a copy! 6: Adhesives, for both mechanical strength and thermal conduction have to be chosen very carefully, after testing for suitability. The dispensing of these adhesives is not a minor problem. 7: Cleaning and cleanliness requirements are not minor, and need attention.

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George S. F. Orsten is a Senior Staff Scientist at Lockheed Missiles and Space Company, Palo Alto, California. He has over 40 years of experience in the design and building of electronic systems and devices. He has been in the space business since 1958 and has served as a member of the Physics and Astronomy Department of the University of Massachusetts for 18 years, doing research and teaching. He has produced many journal articles over the years in the review of scientific instruments, and has given papers at SMI-92 and the International Congress on High-Speed Photography 1960.

Address: Lockheed Missiles and Space Company
3251 Hanover Street, B-251, Dept 97-80
Palo Alto, CA 94304

Lead Finish Comparison of Two Lead Free Solders with 63/37 Sn/Pb Solder Using Wetting Balance, "Dip and Look " Solderability and Board Level Soldering Performance

by

Mark A. Kwoka and Dawn M.Foster
Harris Semiconductor
Melbourne, Florida

ABSTRACT

The use of lead in electronics manufacture will probably be disallowed in the not too distant future. While data is currently being taken regarding the material properties of lead free solders, very little has been published regarding how the new lead free solders will respond to existing methods of solderability assessment. This study will provide an I.C. component lead finish comparison of two selected lead free solders with standard 63/37 Sn/Pb solder using wetting balance and "Dip and Look " solderability test techniques. In addition , an association between board level soldering performance, wetting balance and " Dip and Look " solderability test parameters of the lead free solders will be established.

Introduction

The use of the lead in the electronics industry today accounts for approximately 7% of the total lead consumption(Reference 1). The use of lead in the manufacture of storage batteries accounts for 60% of the total lead produced and is the largest single user of lead(Reference 2). The use of lead is closely regulated in plumbing, paint and gasoline. Currently, the electronics industry has been exempted from the existing requirements regarding lead, but it is increasingly apparent that lead in electronics may well be disallowed in the not too distant future. As a result, efforts have been underway during the last two years to investigate lead free alternatives for interconnection of electronic assemblies. Surveys have been conducted (Reference 1,3) in order to evaluate suitable replacements for 63/37 or 60/40 tin/ lead solder. These surveys have examined many facets of the issue of lead free replacements including the adverse health effects of lead, lead in the environment

and physical and mechanical properties of the lead free replacements. However, there has been little data published regarding the wetting and solderability test performance of lead free termination finish replacements to be used on integrated circuits. In this study, two lead free solder alternatives were chosen for comparison with the standard 63/37 tin/lead solder. Wetting balance, steam age solderability testing and board level soldering performance were chosen as discriminating variables for the comparison.

Experiment

The lead free solders chosen in this study for comparison with 63/37 tin/lead solder were 95/5 tin/antimony and 96.5/3.5 tin/silver. These two solder compositions were chosen as candidates from the survey done by Greg Munie et al(Reference 3) based on the subjectively reported wettability, wetting rate , flux required for soldering and inspectability. 16 lead CERamic Dual Inline Packages with alloy-42 lead frames were acid cleaned with 50% H2SO4 and mixed acids and hot dip processed with each of the candidate solders and the 63/37 control. Three unit samples from each lead finish group were then submitted for Mil Std 883 Method 2003 steam age solderability testing. In addition, wetting balance measurements, using a Kester KS-150 wetting balance, were taken on three unit samples from each lead finish group using the respective candidate solder in the wetting balance test solder pot. The wetting parameters used were T0, T2/3, F@2 sec and T@200 micronewton/mm. Standard weight measurements were also taken on the wetting balance to determine the amount of variability associated with the force values taken on that instrument. Finally, ten units were soldered into three 1 3/4" x 2 1/4" x .055" multilayer circuit boards using O.A. water soluble flux and the respective candidate solders at a temperature of 300 degrees C. No attempt was made to optimize the soldering temperature or determine appropriate preheating for the board level soldering. The resulting solder joints from each composition of solder were then inspected with a stereo microscope at 10X. Due to the small size of the available solder baths, a manual "float" technique was used to do the board soldering. This is, of course, not representative of typical manufacturing conditions but it did produce inspectable board level solder joints The termination finish on the circuit board was a tin lead plating. As a result, the subsequent solder joints that were formed were a mixture of lead free solder along with the lead contained in the finish on the circuit board.

Results and Discussion

The ceramic dual inline packages used in this study were successfully hot dip processed. Elevated temperatures (300 deg C) were used for the hot dip processing of these cerdips with no processing problems noted. It is our opinion that either of these solder compositons could be used with the existing soldering equipment that is currently employed for 63/37 Sn/Pb solder process and would require only minor modifications in the lead finish processing operation for ceramic dual inline packaged integrated circuits. The results of the eight hour steam age solderability testing per Mil Std 883 Method 2003 are given in Table 1.

TABLE 1. Mil Std 883 Method 2003 "Dip and Look" Solderability

Solder Composition	# Defects/# Leads Inspected
95/5 Sn/Sb	0/22 3 units
96.5/3.5 Sn/Ag	0/22 3 units
63/37 Sn/Pb	0/22 3 units

The lead free samples were readily testable for solderability using standard steam age / "dip and look" solderability test techniques. No difference in "dip and look" solderability testing results was observed between the no lead alternative solders and the 63/37 Sn/Pb control.

Wetting balance measurements were used as discriminators in this study. The KS-150 wetting balance used in this study was first characterized via standard weight measurements. This characterization was comprised of repetitive measurements of a known standard weight on the wetting balance over a period of one month to determine the amount of variability associated with force measurements taken on this equipment. Each sampling consisted of 5 repetitve measurements and a mean of those 5 measurements were reported for that day. The rolling range is simply the difference of the current mean and the mean from the previous day. The known weight that was chosen for this task was 4954.8 micronewtons. This weight was chosen because this was within the actual force range that the equipment would be measuring in when the 16 lead CERDIP samples were tested on the wetting balance(assuming reasonably good wetting). The total wetted perimeter of the 16 lead samples is 16(2(0.10) +2(0.20)) (25.4mm/inch) = 24.384mm. Therefore, the

known weight of the sample, expressed as micronewtons/mm, is 4954.8/24.384 = 203.2 micronewton/mm. The purpose of doing this characterization was to estimate the amount of variability associated with the wetting balance itself. This is necessary in order to more clearly understand the effect of the solder composition on the wetting balance parameters. One simple way of characterizing the amount of scatter and accuracy of the measurements taken from this wetting balance, in the range of forces of interest, is in the form of a control chart. The results of this characterization are given in Figures 1 and 2. It is clear that when measuring a force of 203.2 micronewtons/mm on this equipment, we would expect the average of one group of multiple measurements taken on this equipment to be within +/- 12 micronewtons of the true 203.2 micronewton/mm value. As a result, in order to discriminate a difference in wetting forces between solder compositions, a minimum difference in sample averages of 24 micronewtons/mm must be exhibited.

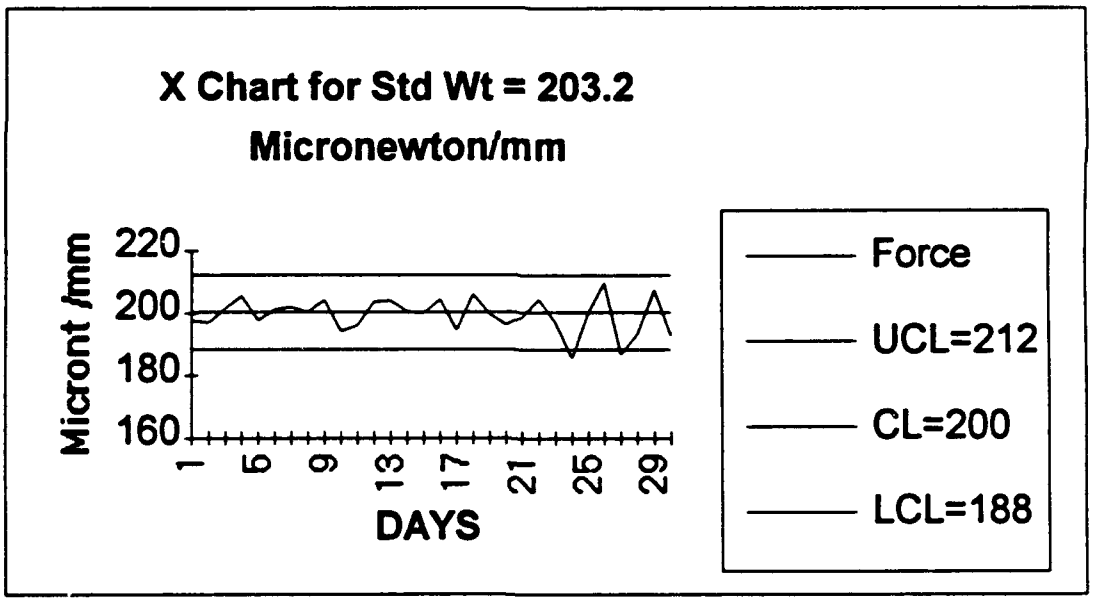

FIGURE 1. X Chart for Standard Weight Measurement
Known Weight = 203.2 Unt/mm

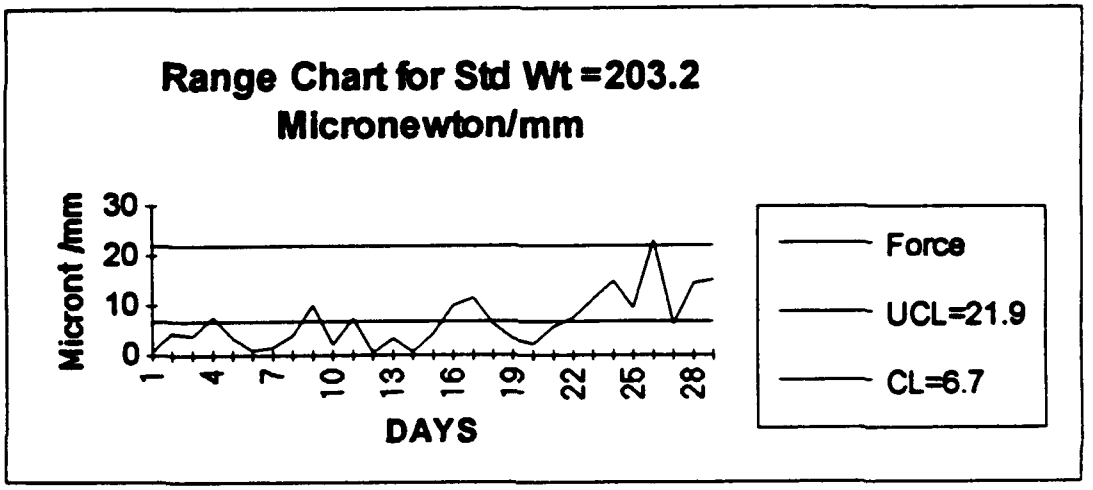

FIGURE 2. Rolling Range Chart for Standard Weight Measurements. N=2

The wetting balance results for the lead free solder alloys compared to the standard 63/37 Sn/Pb solder are given in Table 2.

TABLE 2. Wetting Balance Results for Lead Free Alloys

	T0 (sec)		T 2/3 (sec)		F @ 2 sec		Max Force	
	Xbar	S	Xbar	S	Xbar	S	Xbar	S
Sn/Ag	0.0	0.0	1.23	0.01	549	42	579	47
Sn/Sb	0.11	0.08	0.74	0.07	403	14	413	15
Sn/Pb	0.0	0.0	1.00	0.06	470	24	485	19

Note: N = 3 Testing done @ 300 +/- 5 deg C.

These wetting force values appear too large. The Sn/Pb Max force of 485 micronewton/mm is larger than the 400-420 micronewton/mm value that is typically reported in the industry literature. However this testing was done at 300 deg C. A value of over 480 micronewton/mm was published by R.J. Klein Wassink(4) for 60/40 Sn/Pb solder at 350 deg C in an inert atmosphere. This testing was done in air. Unfortunately, no errors or other assignable causes were determined for these high forces and so they are reported as they were found. A

Duncan/Waller multiple comparisons "T" test was conducted for each wetting balance parameter across the three solder compositions. A statistically significant difference between all three compositions was detected for the T2/3, F@2 sec and Max Force. With respect to wetting forces, F@2 sec and Max Force, the Sn/Ag exhibited the highest wetting forces followed by the Sn/Pb and Sn/Sb, respectively. This pattern however did not carry through regarding the wetting times. The Sn/Ag and Sn/Pb exhibited the same fast wetting speeds,T0=0 seconds, with the Sn/Sb slightly slower at 0.11 sec. The T2/3 however was the fastest for the Sn/Sb which also exhibited the smallest wetting forces. The T2/3 followed an inverse order to the wetting forces with Sn/Sb being the fastest followed by Sn/Pb and Sn/Ag.

The results of the 10 units from each solder composition that were soldered into the three small circuit boards were not discriminating but they were informative. The 63/37 Sn/Pb controls exhibited the "shiniest" top and bottom side fillets of the three solders tested. Also, the 63/37 Sn/Pb solder exhibited the least amount of solder bridges and excess solder on the bottom side of the boards. All three solders exhibited equivalent filleting from a contact angle and circumferential perspective. In all three cases, full top and bottom side fillets were formed. The 63/37 Sn/Pb boards were easily identified and readily categorized by the appearance of the solder joints. However, the 95/5 Sn/Sb and the 96.5/3.5 Sn/Ag could not be discriminated in a blind inspection. Both of these compositions of solder exhibited rough, " grainy " solder joints on both the top and bottom side. Also, both compositions exhibited bridging and excess solder on the bottom side of the boards. No other discriminating factors were discernable. As a result we had no opportunity to employ the discriminant analysis technique in this data set.

Conclusions

In this study we showed that 16 lead ceramic dual inline packages with alloy 42 lead frames can be and infact were successfully hot dip processed with the two lead free solder candidates 95/5 Sn/Sb and 96.5/3.5 Sn/Ag at 300 degrees C. Also, it is likely that these two lead free solders could easily be used as "drop in" replacements for the current Sn/Pb solders for the termination finish processing of ceramic dual inline packaged integrated circuits with minimal equipment/process modifications. "Dip and look" steam age solderability testing can be done on ceramic dual inline packaged integrated circuits with hot dip Sn/Sb and Sn/Ag termination finishes with no difference in solderability test results on properly

precleaned units compared with the respective 63/37 Sn/Pb controls. Samples of units from all three solders tested in this study passed the 8 hr steam age test and also produced acceptable solder joints on the assembled circuit boards.The wetting balance equipment used in this study exhibited variability in average force measurements of approximately +/- 12 micronewtons/mm over time. This scatter is due to the wetting balance equipment itself. Unusually high wetting forces were measured during this study, perhaps due to the elevated temperature(300 deg C) used during the wetting balance testing. A statistically significant difference in the wetting forces F@2 sec and Max Force was measured among all three solders tested. The Sn/Ag exhibited the highest wetting forces followed by the Sn/Pb followed by the Sn/Sb. All three solders exhibited fast wetting speeds of less than 0.12 seconds. The time to 2/3 max force, T2/3, was also significantly different among the three solders. The Sn/Sb exhibited the fastest time followed by the Sn/Pb and then the Sn/Ag. This is unusual in that usually the samples with the largest F@2 sec also have the fastest wetting speeds. The board level soldering results were not discriminating enough to establish an association between the wetting balance and "dip and look" testing with the board level soldering performance as originally intended, however the results were informative. Small, .055" thick circuit boards were successfully soldered with lead free solder alternatives at elevated temperature(300 deg C) with no visible damage(burning) to the circuit board. Full topside fillets were observed on the finished boards that were soldered with the lead free alternatives. Extremely rough surfaced fillets on both sides and bridging/excess solder on the bottom side of the boards soldered with the lead free alternatives were observed. The 63/37 Sn/Pb solder produced the best board level solder joints in this study. No clear difference in board level soldering performance was exhibited by either of the lead free solders evaluated in this study. As a result of the higher wetting forces and the improved resistance to poisoning from Pb, the 96.5/3.5 Sn/Ag will be further evaluated in a follow up study on plastic dual inline packages with copper lead frames.

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Mark Kwoka is a Staff Engineer (lead finish) at Harris Semiconductor and has been with Harris for the past 10 years. He has served as the sustaining engineer for the matte tin plating, component soldering, and module surface mount assembly process lines, and currently is responsible for worldwide lead finish process development, lead finish quality, and solderability of all analog and digital products.

Mark became a certified electroplater-finished (CEF) in 1983. He was issued his first U.S. Government patent for matte tin reflow processing in 1987. He was issued his second patent in 1989 for leadless chip carrier soldering. Mark has published and presented five technical papers on soldering and solderability testing (883/38510, etc.) and has lead IPC seminar/workshop and discussion groups on solderability testing.

Mark holds a B.S. degree in Chemistry from the University of South Florida and an M.A. degree in Chemical Engineering from Purdue University. He is Chairman of the EIA Soldering Technology Committee and is Cochairman of the Joint IPC/EIA Task Group drafting the ANSI/J-STD-002 Solderability Test Method. Mark is also a member of the U.S. Technical Advisory Group TC-91 WG 3, the IPC Steam Age/Solderability Task Group, the IPC Accelerated Aging Task Group, and the IPC Wetting Balance Task Group.

Address: Harris Semiconductor
P. O. Box 883
Melbourne, FL 32901-0101

An Examination of the No-Clean Soldering Process

By

Debra Kopp
Integrated Technologies Group
Durham, NH 03824
(603) 868-1754

Phil Zarrow
GSS/Array Technology
San Jose, CA / Durham, NH
(603) 868-1967

Introduction

The no-clean soldering process is gaining momentum as a viable method for achieving electronic assembly without the use of CFC-containing solvents in compliance with the Montreal Protocol. The no-clean process has been successfully adapted to hand soldering, wave-soldering, and reflow soldering. While this report focuses on no-clean solder pastes for reflow soldering, the concept and many of the nuances are applicable to flow soldering and hand soldering as well.

A no-clean process can be a matter of using a rosin-based flux and simply not cleaning the PCB assembly. In reality, this type of no-clean process has been used for years on certain consumer electronic products (for example, Japanese television sets). After soldering, the activators in these RA and RMA fluxes are encapsulated by the residue. It is better to not clean at all than risk disturbing the containment of the activators in an insufficient cleaning process. The PCB assemblies are never seen by the end-user so aesthetics is not an issue. Of course, these products reside in very "comfortable" environments where extremes of temperature and humidity are not present to promote corrosivity.

In today's context, no-clean soldering refers to printed circuit board assemblies soldered in a manner such that little or no flux residue or other contaminants are left on the assembly, thus making the cleaning operation unnecessary. This objective is achieved through the use of either a "fluxless" or low-residue soldering process.

No-Clean Solder Paste

No-clean solder pastes can be classified into four categories: standard no-cleans, low residue no-cleans, very low residue no-cleans and ultralow residue no-clean pastes. These can be further subclassified into rosin based and non-rosin based. Table 1 summarizes the characteristics of the different no-clean classifications.

Standard No-Clean Pastes. Standard no-clean pastes are typically rosin based and have a solids content between 3.5% and 5.0% by weight. Residue content and color vary between suppliers but the typical color is clear to yellow. While clear residues are desirable for aesthetic reasons, residue color has no bearing upon corrosivity and resulting reliability of the PCB assembly. Standard no-clean pastes do not require a special atmosphere such as nitrogen for reflow and joint solderability is typically good to excellent. Although wetting has been cited as an issue with no-clean pastes, the problem is usually attributed to poor solderability of the components and substrates. Since the standard no-clean pastes are mostly rosin based, the tack times and print characteristics are comparable to the range of RMA (solvent-cleanable) and OA (water-soluble) pastes that many users have had experience with. Major drawbacks to the standard no-clean pastes are the color and quantity of residue. Yellow residues may be cosmetically unacceptable to users; excessive residue may impede "bed-of-nails" in-circuit testing.

Low Residue No-clean Pastes. Low residue no-clean solder pastes can be either rosin or synthetic based. Typically the pastes with the lowest residue level use synthetic non-rosin-based ingredients. The main advantage of the low residue pastes is the reduced residue levels, which inherently diminish cosmetic concerns as well as reduce and even eliminate probing problems with "bed-of-nails" testing. Solids levels range from approximately 3.4% (by weight) in low residue formulations, to 2.1% to approximately 2.8% for very low residue solder pastes, to less than 2% in ultralow residue pastes. The percentages vary among vendors, but the trend among the suppliers is to produce effective formulations with lower residue levels.

Low, very low and ultralow residue solder pastes are typically formulated by raising the metal content to 91 - 92% (hence reducing the flux content by as much as 20%) as well as by designing a flux that will largely decompose or vaporize during reflow and thus reduce the resulting residue. As a result of both a higher metal content and, sometimes, a higher concentration of solvent in the flux system, tack times and work life for low residue no-clean pastes may be considerably shorter than what has been experienced with standard RMAs and OAs.

The low residue no-clean flux formulations tend to be less chemically aggressive than the RMAs and OAs most users are accustomed to.

Applied No-Clean Soldering Process

A number of factors are driving many users to consider incorporating the use of no-clean solder pastes into their products.

Reduction of Manufacturing Cost. In terms of machine centers, incorporation of no-clean pastes into the assembly process allows the cleaning system and possibly the water treatment system to be eliminated. Successful implementation of no-clean soldering in existing and newer applications will likely preclude the purchase of new cleaning systems on future lines and subsequent utility requirements (for example, water treatment, heating, and plumbing).

Elimination of the cleaning process center reduces the cost of producing each PCB. This reduction is achieved through an aggregate savings in processing time, materials, water pre- and post-treatment, overall power consumption, set-up, and operating manpower.

In terms of material cost, variation in solder paste price is primarily a factor of particle size and metal alloys. Hence, the use of a no-clean as opposed to an OA or RMA flux should not substantially affect the cost of the solder paste.

Compliance with Bellcore Specifications. Bellcore compliance is mandatory for many communications products. A number of RMA fluxes are available that comply with Bellcore specifications, but their use would require either solvent (CFC-113) cleaning or the use of a saponifier in the aqueous cleaning process. Water soluble (Organic Activated) solder pastes do not meet Bellcore specifications. However, a number of very-low residue no-clean pastes do comply with these specifications. Therefore the no-clean process can be a viable solution to elimination of CFCs.

Environmentally "Greener" Process. Elimination of both CFC-113 solvent and aqueous cleaning processes has an obvious positive environmental impact. The problem of solvent disposal and water treatment and disposal is eliminated and, hence, the overall waste stream is minimized. In addition, concerns over VOC and other emissions from the cleaning agent are eliminated. Solder paste manufacturers claim that no-clean pastes do not appear to produce any higher or more toxic emissions than RMA flux formulations.

No-Clean Process Concerns

Ideally, the incorporation of a no-clean solder paste into a product build should be transparent to the process (aside from "turning off the cleaner"). In reality, as high-reliability products are being manufactured, it is essential that the prospective low residue solder pastes be evaluated in terms of their impact on product manufacturability and reliability.

Manufacturability. Substituting the selected no-clean paste should not affect the manufacturing process; hence the paste should maintain as many of the characteristics of the RMA or OA pastes already being used in the process. Ideally, machine set-up parameters, such as stencil printer adjustments and reflow system speed and emitter settings, should not be different between the two paste types.

Solderability. Solderability is defined as the ability of a metal to be wetted by molten solder. In the context of evaluation of no-clean pastes, the solderability tests include testing for cumulative solder balls as well as testing of the wetting ability of the solder paste.

Solder balls are small spherical particles of solder, approximately 0.002" to 0.005" in diameter, that reside on the nonmetallic surfaces of the substrate. They are caused by very fine powder particles in the solder paste that are carried away from the main solder deposit as the flux melts and flows prior to the solder itself melting. Solder balls can be formed by solder deposition off the land pad (as a result of bad stencil design or misregistration). In addition, they can be formed when the oxide layer on the surface of the solder powder particles is so thick that the flux and other activators in the paste are not aggressive enough to remove it, and is separated from the main mass of oxide-free solder. Factors such as improper solder paste storage and incorrect reflow profile can increase the likelihood of solder ball occurrence; however, assuming that these process parameters are controlled, the oxide content and the tendency to ball can be indicative of the quality of the solder paste. In a process where the soldered assemblies are cleaned, solder balls tend to be washed away. However, in a no-clean process, solder balls that have formed will reside on the board and the mobile ones can become a reliability hazard as potential shorting conductors.

The wetting test helps determine whether the flux is aggressive enough to reduce the oxide layer enough for the solder to adhere to the surfaces so that a good metallurgical bond has formed. In an evaluation procedure, a good bond is indicated by the angle of contact of the solder on the base metal. A smaller contact angle is indicative of better attraction and a resulting stronger bond. A larger contact angle indicates a superficial attraction between the surfaces, resulting in a weak joint.

Work Life. The working life of a solder paste is the length of time the paste can be left without degradation of its rheological properties on the stencil before printing as well as on the substrate after printing. Of the two, the time that the solder paste can reside on the substrate prior to reflow is more important. That time defines parameters within the process including how long the placement machine has to place components into the paste as well as how long substrates can be "buffered" before placement and before reflow. Delays in assembly (for example, change of shift, stalling or breakdown of the placement or reflow systems) will also affect the working life of the solder paste.

An evaluation procedure should examine the tackiness of the subject solder pastes. Tackiness is the ability of the solder paste to hold the SMCs in place after placement prior to reflow soldering. Failure of a tackiness test indicates that the useful working life of the solder paste has expired.

While controlled production planning and scheduling as well as well-maintained equipment will help ensure reflow within the work life of the paste, the unplanned can and does happen. A work life of 4 hours should allow a good margin of safety for most manufacturing lines.

Performance Characteristics. The performance of the solder paste is examined in two categories: printability and solder joint appearance. Printability is important because the no-clean solder paste must handle a wide range of lead pitches. Ideally, a paste should not spread during the reflow process to the extent of inducing bridging between adjacent interconnections.

Printability of a solder paste is reflected in the accuracy and reproducibility of the stenciled solder paste pattern onto the land patterns. Slump is the ability of the paste to spread out after being deposited on the pads; it should be minimal. Slump is affected by the percentage of metal in the paste. Because no-clean solder pastes typically have higher metal contents than standard RMAs and OAs, some no-clean pastes are incompatible with fine-pitch lead spacing as excessive slump will lead to bridging.

A certain degree of slump will be present in the paste at ambient temperature, and this will be examined in a printing and slump test. As the paste is heated and solvents and rheology modifiers are driven off, the paste may tend to slump further, perhaps beyond allowable limits, to the degree where metal surface tension will not amply pull it back in again. Thus, in an evaluation, the slump characteristics (spread) should be examined after preheat temperatures are realized (approximately 100° C) as well as after preflow (approximately 160° C).

Reflow Profile. The reflow profile is a recipe of temperature and time durations that the solder paste is subjected to in the mass reflow system. These parameters are dictated by the chemistry and the metallurgy of the solder paste. The reflow profile is composed of four zones: preheat, preflow, reflow and cooldown. While there is generally a fairly decent operating envelope to the profile, this envelope can be expected to tighten up with the use of no-clean pastes. Higher metal content will affect soak times, as will the various rheology modifiers and

solvents. The minimum peak temperature that must be attained (full liquidus temperature) should not be so high (for the no-clean formulations) that PCB assemblies will be exposed to extremely high temperatures for long durations.

Materials Intercompatibility. It is important that the chemical composition of the no-clean solder paste be benign in that it does not react with other materials on the assembly.

Solder Mask. While there have been some problems with liquid no-clean fluxes (wave-soldering process) reacting with some solder mask material, there does not appear to be any documented occurrences of no-clean solder paste chemistries interfering with solder masks. This, however, assumes that the solder mask has been properly applied to the substrate and cured per the manufacturer's specifications.

Conformal Coatings. If an application uses a conformal coating, there must be compatibility between the coating and the no-clean flux chemistries. Possible degradation is determined by measurement of surface insulation resistance (S.I.R.), taken both before and after thermal cycling in a temperature/humidity chamber. In addition, a test should be done to determine whether the adhesion properties of the conformal coating are adversely affected by the presence of no-clean flux residue on the assembly.

Other Fluxes. Conformal coatings and solder masks are not the only additional chemicals that may be placed on the assembly that have the potential for reaction with the no-clean residue. Rework of the assembly is a "fact of life" which involves replacing and resoldering a component to the assembly. Typically, this a manual operation that involves the addition of liquid flux to the replaced component and its lands onto the substrate. That flux should not introduce adverse effects and, thus, should be compatible with the no-clean paste chemistry. Such adverse reactions observed in the industry have included excessive corrosiveness and degradation of conformal coating.

Testability. Leaving a flux residue on the PCB assembly has the potential for interfering with bed-of-nails testing. The residue acts as an insulator that can prevent the probe from making proper electrical contact with the testpoint. In addition, some flux residues have been observed to accumulate on the probe as well, leading to contact failure. This is another reason for the drive towards ultralow residue no-clean fluxes.

Reliability. As stated earlier, beyond the manufacturing process the reliability of a product is related to the environment it will reside in. Current available data indicate that products assembled with no-clean solder pastes that are subject to "mild" environments, in terms of thermal extremes and humidity, have done well. However, because of the relative "newness" of no-clean soldering in the present context, very little reliability data are available. It should be noted that very high reliability applications such as military, aerospace and medical electronics have shied away from considering no-clean processes. Many industrial, computer, and consumer electronics applications, which are subject to moderate temperatures and humidity, are prime candidates for this process.

It is recommended that, as part of real-life testing, actual trial applications be subjected to reliability testing. Thermal cycling corresponding to the range of the application's environment would be a primary evaluation tool.

The Nitrogen Question

Heat is a catalyst for oxidation, and some of the no-clean solders perform better in an inert oven where the reflow process is not compounding oxidation of the PCB assembly. The required nitrogen level depends upon the vendor and the solids content of the specific paste. It can range from 1,000 ppm oxygen to as low as 10 ppm oxygen. Nitrogen use increases the cost of the manufacturing process. Reflow ovens equipped for inert atmosphere are more expensive than their nonatmosphere-contained counterparts. Retrofitting atmosphere containment capability to existing ovens is not effective, as these modifications seldom attain levels of less than 1,000 ppm oxygen. The facilities, if not already set up and plumbed for nitrogen, would also have to be modified. More important is the on-going process cost. In spite of the fact that running a no-clean process with nitrogen would still cost less than the aqueous cleaning process currently does, this cost, facility, and process concern would best be avoided. Upon close examination, it currently appears that only the ultralow residue pastes actually require an inert atmosphere during reflow.

Conclusion

The no-clean process is not a panacea and is therefore not suitable for all SMT applications. The tightening of manufacturing process parameters must be addressed. In addition, thorough testing should be done in order to comprehensively evaluate the no-clean process in the assembly process.

It must be understood that the process envelope has narrowed with the incorporation of no-clean solder pastes. It is, therefore, not a totally drop-in manufacturing process. For example, cleanliness throughout the process has to be maintained more diligently, especially with regard to incoming components and substrates. This will involve interaction with the suppliers. Changes made to the assembly process should also be understood by all concerned.

The user must also understand the implications of the no-clean process. With the initial real-life testing trial period, some applications may experience higher field failures, reflecting upon the requirement for adjustment of the process and/or materials. The aesthetic considerations must also be taken into account. These considerations are somewhat of a marketing question.

The realized positive aspects cannot be overstressed. They include the lower cost of assembly and the fact that the process is environmentally friendlier than other alternatives.

The no-clean process has been successfully implemented worldwide. The major driving force is that it is being recognized as the ideal process to address the CFC issue while also achieving substantial manufacturing cost savings.

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No-Clean Solder Paste Type	**Solids Content** (by weight)	**Atmosphere**
Standard	3.5 - 5.0%	Air
Low residue	2.9 - 3.4%	Air; nitrogen levels of 500 ppm O_2 may improve wetting
Very low residue	2.1 - 2.8%	Air; Nitrogen levels of ≤500 ppm O_2 sometimes recommended to achieve better wetting
Ultralow residue	< 2.0%	Nitrogen < 100 ppm O_2 required

***Table 1*: No-clean solder paste classification.**

Debra Kopp is currently working for Litton Amecom's Space Systems Operation in College Park, Maryland, as a Principal Member of the Technical Staff. Her career has included production process support, process development, and solder joint reliability research.

Debra has a B.S. degree in Industrial Engineering from Arizona State University and an M.S. degree in Industrial Engineering from Stanford University. Her work in the electronics industry has earned her a listing in "Who's Who in Science and Engineering."

Debra has authored and presented numerous technical papers on SMT-related topics and has both chaired and presented at key technical conferences and seminars. She is a member of the IPC's SMT assembly reliability committees, the Surface Mount Technology Association, ISHM, and IEEE, and is a senior member of the Institute of Industrial Engineering. She is a partner and cofounder of the Integrated Technologies Group.

Address: Integrated Technologies Group
Durham, NH 03824

Phil Zarrow has been involved with hybrid and PCB assembly for over 18 years. He has worked with equipment for circuit board fabrication and assembly of through-hole and surface-mount technologies. In addition to his background in automated assembly and cleaning, he has extensive experience in SMT placement and reflow soldering. In his position as Manager of Technology Development for GSS/Array Technology, a major contract assembly firm, Phil is responsible for examining and working with emerging and leading-edge technologies, equipment, and processes.

Phil has chaired and presented at numerous seminars and conferences and has published many technical papers and magazine articles. He is a member of IEEE, SME, and ISME, and is a partner and cofounder of the Integrated Technologies Group (ITG). He is past national director of the Surface Mount Technology Association (SMTA); an instructor and advisory council member for the National Training Center for Microelectronics; and a past chairman of the Reflow Committee for SMEMA. Phil serves on the Editorial Advisory Board of *Circuits Assembly* magazine.

Address: Integrated Technologies Group
Durham, NH 03824

CLEANED LOW SOLIDS/NO CLEAN FLUXES ON HIGH RELIABILITY HARDWARE

by

Patrick Scott, Ed Hauptfliesch, Philipp Schuessler, Randy Long
Process and Materials Engineering
IBM/FSC
Owego, NY

ABSTRACT

In this project cleanable LS/NC fluxes are evaluated for the various solder processes associated with high reliability avionics assemblies. Ionic and non-ionic residual contamination, surface insulation resistance (SIR), ease of cleaning, solder penetration/wetting and metallurgical cross sections are the variables monitored and optimized. The reliability of some solder processes, as measured with ionic contamination and SIR test, is comparable with rosin (RMA) flux soldered assemblies. LS/NC flux which is not completely thermally treated by the solder process does remain active as measured by ionic contamination test and decreased SIR performance. Treating these active residues with a suitable bakeout volatilizes residual flux residues and yields acceptable ionic and SIR performance. Cleaning the no clean flux processed assemblies enhances the results even further. The data thus generated shall be used in contract negotiations to eliminate ozone depleting chemical (ODC) cleaning processes.

INTRODUCTION/GOAL

Chlorofluorocarbon 112, 113 and methyl chloroform are eliminated from IBM/FSC Owego through the use of 2-propyl alcohol (IPA) and HCFC-141b/methanol blends on the high reliability space and military avionics assemblies IBM/FSC produces. The tally as of this printing is seven in-house designed and built IPA cleaners and seven HCFC vapor degreasers. This represents significant improvement from the forty-four vapor degreasers that once occupied the facility and the numerous methyl chloroform based operations conducted in house and at vendors. To date approximately $2.1 million of ozone depleting solvents have been saved at IBM/FSC Owego alone.

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The goal of this work is to reduce the alcohol cleaning cycles to (ideally) one prior to conformal coat, and to completely eliminate the use of HCFC-141b blends from mass reflow solder cleaning. The reliability effects of cleaning and cleaning process failures is evaluated through the use of ionic contamination and surface insulation resistance (SIR) testing. The other parameters evaluated in the study are solderability (and solder penetration), metallurgy and conformal coat interactions. The negative effects of glycol based hot air solder level fluxes on epoxy boards is demonstrated once again.

An additional discussion on the contract waivers and negotiations required to convert from rosin flux chemistry is also included.

APPROACH TO FLUX SELECTION

The transition to non-rosin fluxes on high reliability hardware is a significant step. The benign nature of rosin and RMA fluxes gives the high reliability community a security blanket such that any manufacturers using poorly controlled cleaning processes should be able to produce hardware without long term reliability concerns. It is felt and has been repeatedly demonstrated (Reference 1) that if properly formulated and utilized RMA fluxes are left behind by the cleaning process, no detrimental factors are introduced.

One option is to switch to a typical water soluble flux (WSF). This however requires proof that the cleaning process employed is effective and controllable. In-process verification is not usually accurate using conventional means (i.e. ionic contamination testing) on high geometry hardware with close tolerances. The second option is to guarantee that the flux residues left behind are as benign (or may be rendered as benign) as the rosin flux residues they are replacing.

Obviously it is most desirable to have flux residues that are as benign as the rosin residues. If it can be proven that the flux residues are benign then extensive process control, difficult (or impossible) verification is not as critical, and the danger of a process control escape causing reliability concerns is greatly reduced.

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The most logical step in non-rosin flux selection is to pursue low solids/no clean (LS/NC) technology which the commercial electronics industry has used for years. When the additional steps which contribute to reliability (reduced cleaning - when compared to rosin, plus bakeout of residues) are performed the benign nature of rosin fluxes may again be attained. In particular, it is desirable to select a LS/NC flux system which is cleanable in non ODC solvents (water and/or alcohol) and which vaporizes at non-damaging temperatures to allow follow up bakeouts to thoroughly remove residues from hard to clean locations. It is a key parameter that the LS/NC flux selected be cleanable since general nonflux process residues (fingerprints, debris, etc.) shall always be a concern when high reliability, conformal coated assemblies are being manufactured. One cleaning step may be adequate and required (Reference 2) to remove these residues (plus any cosmetic LS/NC flux residues), give good ionic cleanliness and conformal coat adhesion.

The flux selection therefore has the following criteria that are essential to successful and reliable implementation of a low solids/no clean flux soldering program: (1) Ease of cleaning; (2) Solderability; (3) Metallurgy; (4) Surface Insulation Resistance (SIR); (5) No Adverse Conformal Coat Reactions.

The flux selected is based on an organic acid which volatilizes at solder temperatures. The organic acid is present in low amounts to minimize potentially reactive residues left on the assembly.

The following sections elaborate on the above performance requirements and the corresponding test results.

EASE OF CLEANING

Any fluxes chosen for evaluation must be cleanable in water and/or alcohol to allow cleaning & deionized water rinsing prior to conformal coating. This cleaning must remove visual (but hopefully benign) solder flux residues and other production contaminants (hand oils, salts, silicones, etc.) that may interfere with conformal coating or affect reliability. Any fluxes which utilize binding resins to encapsulate the active residues are not considered.

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The primary requirement is that cleaned, soldered assemblies must pass MIL-P-28809 ionic contamination testing as outlined in internal operating procedures using commercial ionic contamination test equipment. Cleaning per the standard in-house clean with isopropyl alcohol followed by deionized water rinsing per internal documentation is allowed. An evaluation of uncleaned, soldered assemblies ionic contamination levels is recorded for information purposes only. Ionic contamination failure may be caused by inadvertent handling of the assembly, not necessarily the flux. Every attempt is made to pass ionic contamination test without cleaning, but failure of the test without cleaning does not constitute failure of the flux or solder process.

CLEANING RESULTS

The flux selected may leave a fine white residue if applied properly. If applied in excess the residue looks like the white residues that plague production lines utilizing rosin based fluxes. When washed in 150 - 160°F water these residues are removable, however, occasional brushing is required.

When several different assemblies were sprayed with excess flux and wave soldered the assemblies passed ionic contamination testing. However, when flux was applied to the board after wave solder (to simulate rework or hand solder) the results were drastically different. Apparently, the flux had volatilized or neutralized to the extent that the ionizable (acid) portion was removed during wave solder, however subsequent additions of flux left "raw" organic acids which were ionizable and conductive in the test solution. Thus leaving unheated LS/NC flux on the assembly left residues which were readily detectable in ionic contamination test.

It was noted in the course of testing that the flux could be neutralized by excessive preheat prior to wave solder. In these cases the boards behaved as if there was no flux applied. This data point was used to hypothesize that the "raw" rework flux (excess flux applied to the touch up area) could be neutralized or volatilized by a follow up bake cycle. Figure 1 shows a comparison of ionic contamination test results for wave soldered assemblies, assemblies treated with raw

flux, assemblies treated with raw flux followed by bake cycle 1 and raw flux followed by bake cycle 2. A very important data point to this study was that the flux could be made to pass ionic contamination test by a bake cycle that is within the temperature range of the assembly and not excessively long in dwell. Figure 1 also shows the expected positive effect of an alcohol clean followed by a deionized water rinse.

SOLDERABILITY

No decrease in the solder joint quality is permitted when the transition to the LS/NC flux is made. Solder penetration, heel fillets and wetting must be equivalent to, or better than the solder joints made with RMA fluxes. The IBM/FSC Owego Workmanship Standard defines requirements for all types of solder connections made in the facility and is used as the guide for quality-no-clean flux solder connections. Solder penetration for pin in hole connections shall be in accordance with the specifications for the various programs, board configurations and thicknesses (0.144" - 0.220").

SOLDERABILITY RESULTS

All hand soldering experiments with the flux were successful provided that the operator understood the differences in technique when using a LS/NC as opposed to a rosin based flux. In some cases the flux would be volatilized prior to the solder connection leading to icicles and poor wetting. However with additional practice all operators involved in the evaluation were capable of making adequate connections using the new material.

Wave and dip soldered assemblies had decreased icicles and bridging when compared to rosin, but the surface of the joint was not as aesthetically pleasing (shiny and smooth). Figure 2 shows the solder penetration that occurred on three key IBM/FSC Owego programs. In one case the board was 0.180" thick, had considerable heat load due to circuit density but still had, excellent penetration. The second board was 0.220" thick and had less than expected solder penetration. Follow up testing and analysis revealed that the RMA flux could not perform any better than the LS/NC because the test assembly was manufactured from a scrap

mother board that was rejected for poor solder plate in the PTH barrels. The third set of boards on Figure 2 were immersion tinned prior to wave solder and 0.144" thick. Again, the penetration is acceptable.

Infra red soldered assemblies had good wetting and heel fillets and were in accordance with the workmanship standard.

Additional work must be performed regarding wave solder preheat cycles which had to be reduced in order to keep from neutralizing the flux prior to reaching solder temperatures. The profiles must be checked against the thermal shock limitations for the various programs.

METALLURGICAL REQUIREMENTS

Cross sectional analysis of soldered connections must show no variances from the standard metallurgical connections associated with RMA fluxes currently in use. Pull strengths of lap joint soldered connections must be insignificantly different than connections made with RMA fluxes if they are necessary to evaluate the particular solder connection.

METALLURGICAL RESULTS

All soldered connections in IBM Owego are made to tinned components and hot air solder leveled (HASL'd) or immersion tinned boards so the metallurgical analysis requirements are somewhat of a moot point because the metallic interface is formed prior to LS/NC flux use. However, all results of typical pin in hole solder connections on HASL'd and immersion tinned boards had little to no voiding, good wetting to all surfaces and good intermetallic formation.

SIR REQUIREMENTS

Surface Insulation resistance of IPC-B-36 test coupons shall be approximately equivalent to those associated with the current rosin fluxes when the fluxes are placed on the test coupons and subjected to the soldering and cleaning profiles that production

hardware shall see. Assemblies shall be tested in uncoated, cleaned and baked condition. All of the specific board materials that may be subjected to the given solder process (epoxy and polyimide) shall be used in the construction of the IPC-B-36 test coupons. Testing shall be in accordance with IPC-TR-580 and shall follow the humidity, temperature, voltage bias, and measurement requirements therein.

Flux and solder process qualification shall be in accordance with the requirements of MIL-STD-2000A. This requirement calls for 24 IPC-B-26 coupons to be subjected to the solder, clean and coat process of record. The test requirement of MIL-I-46058 shall be imposed on the assembly. The daisy chain LCC patterns shall read 100 megohms at the high humidity portion of the test, and 5000 megohms within 24 hours of the high humidity portion of the test.

SIR RESULTS

SIR was determined to be the most relevant test of the long term reliability of the flux, solder and cleaning process. In this study the goal was to see how well the system would perform in the event of cleaning process failures. The initial data presented here focused on the extremes of thermal input which assemblies were exposed, i.e., wave solder and hand solder respectively. In the case of wave solder the entire assembly was heated to solder temperatures. In the hand solder situation only the solder connection would be heated to temperatures high enough to volatilize the flux. The remainder of the board may have excess flux applied to it which is active and potentially damaging. In order to simulate the unheated zones of a hand soldered assembly the board was sprayed with flux on both sides and tested. When baking experiments were conducted both sides of the board were sprayed with flux prior to the bake operation.

Figure 3 shows the SIR results for various conditions of flux application and thermal input on polyimide IPC-B-36 boards.
The key results and data points are as follows:

1. The SIR of boards with LS/NC flux applied to both sides, wave soldered and without cleaning was within

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1.5 decades of RMA fluxed, waved and cleaned boards.

2. "Raw" LS/NC flux is very detrimental to board performance causing massive SIR decline and visible corrosion products.

3. Baking the LS/NC flux after application to the HASL'd board brought the SIR reading above the RMA soldered & cleaned assembly to almost the value of the baseline (HASL only) board.

This key breakthrough implies that cleaning process failures would not cause flux related reliability problems provided that a proper bake operation is performed prior to application of conformal coating. Even without cleaning the benign nature of rosin fluxes may be guaranteed with a simple bake step when working with polyimide boards.

Figure 4 shows the results of a similar test matrix for epoxy IPC boards. In this case the results require further discussion and testing. The key points are:

1. The bake process as applied to IPC-B-36 boards sprayed with LS/NC flux does keep the SIR results above the 10^7 ohm/square limit of MIL-P-55110D.

2. The wave process did not prove out well with the LS/NC flux. The SIR dropped considerably below the limit and remained flat (cell not shown on graph).

3. The last three cells in Figure 4 were not HASL'd with water soluble flux, the assemblies were glycol free and in all cases (wave solder with LS/NC, baked with LS/NC and the control group) the performance was 2-4 orders of magnitude higher. This is in accordance with published literature (Reference 3).

A significant factor was certainly the glycol based water soluble flux that was used to HASL the B-36 boards prior to SIR test. Figure 5 shows a spectra of the shiny film noted on the surface of the epoxy board following SIR testing as compared to the water soluble HASL flux used by the board supplier. The spectra positively identifies the contamination as the HASL flux. Only barely detectable amounts were found on the polyimide boards.

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CONFORMAL COAT EFFECT REQUIREMENTS

The LS/NC flux must not interact adversely with coating to cause reversion, peeling or any other detrimental effect that may occur with conformal coating. The testing shall involve leaving flux on the assembly prior to coating in one test. In the other test the bakeout shall be performed on an assembly that has had the flux applied.

CONFORMAL COAT TEST RESULTS

In the example where the coating was applied over fluxed surfaces dewet occurred eliminating any need for discussion of flaking, peeling, etc. effects. In the case where the assembly was baked prior to application of the conformal coat all flux residues had been removed and the coating behaved as expected. This fluxed, baked, and coated IPC-B-36 assembly was subject to the SIR test with positive results. The SIR data was well within the range of the rosin and untreated control groups.

SURFACE ANALYSIS STUDY ON EFFECTS OF BAKING FLUXED ASSEMBLIES

The fact that baking dramatically improves the results of ionic contamination and SIR tests of LS/NC treated assemblies is a very interesting starting point for near guaranteed reliability on MIL-Spec hardware. It is however necessary to understand the mechanism of this "neutralization" of the flux from SIR and ionic contamination test vehicles through the solder process heat or a controlled post solder bake step.

Figure 6 shows the Fourier Transform Infra Red (FTIR) spectra of the flux applied to a salt flat and baked 1 hour and 4 hours. Note that after 4 hours the spectra is void of absorption peaks. The evidence is that the material had not transformed, but had completely sublimed. The positive implication is that no flux breakdown products remain on the board provided that the appropriate thermal treatment has been applied. The negative aspect is that diffusion hindrances may make the bake cycles necessary to remove "raw" flux from plated through holes, circuit board to heat sink bondlines, etc. unacceptably long or ineffective. Further testing is required along this avenue.

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SUMMARY/CONCLUSIONS

The results of this study indicate that implementation of cleanable low solids/no clean fluxes on high reliability is entirely feasible. The flux evaluated volatilizes at mass reflow solder temperatures (wave, dip & IR solder) leaving the assembly with no active residues as measured by ionic contamination and SIR testing. Utilization of the LS/NC flux on resistance soldering processes that heat only the solder connection area (hand solder, hot bar, etc.) may create reliability concerns because the entire area fluxed may not be sufficiently heated to thoroughly volatilize the flux. The active acid residues show up in ionic contamination test and cause dendritic growth and corrosion products during SIR test on polyimide IPC-B-36 test boards. These residues may be removed by a bake operation that is within the safe temperature range of production assemblies and not unacceptably lengthy. Baking the test boards following flux application brought the SIR results up to the values of the control boards (rosin fluxed, soldered and cleaned in HCFC, alcohol and water). Epoxy IPC-B-36 SIR testing was confounded by the use of a glycol based hot air solder leveling flux that lowered SIR by 4 order of magnitude. Dendritic growth and corrosion occurred in many of the test cells which had no ill effects on the polyimide counterparts. Eliminating the WSF flux gave SIR performance similar to polyimide boards and assemblies - well above the 10^7 required by MIL-P-55110. Implementation and qualification testing of the new flux is currently underway for 1994 production.

COMPLIANCE TO CONTRACTS AND REGULATIONS

The forgoing discussion provided insight as to how a Department of Defense Original Equipment Manufacturer (DoD/OEM) resolved the problem of CFC/ODC elimination. However, the legal or contractual obligations remain, in part, to be satisfied in accordance with Federal Aquisition Regulations, military specifications and military standards. As defined in the specifications, one cannot deviate from an agreed upon, well defined manufacturing process unless the customer provides written approval in advance of product being shipped. Furthermore, when a large OEM has in excess of 1000 open contracts and purchase orders in various stages of completion, it becomes a logistics nightmare to meet

every contractual requirement and federal ruling. The problem is further complicated by the introduction of public law 102-484 which stipulates that, under specific conditions, no contract, dated after June 1, 1993 will require CFC/ODC free processes. This leads one to conclude that dual cleaning processes must now be implemented. In addition, IBM/FSC, as well as other OEMs are now being requested to supply assurances of being ODC free, and to assure that even subcontractors are equally compliant. These requests, unfortunately lie outside the scope of the regulations and public law. The net result is added cost for the OEM to generate the information and pass it along to the customer. Fortunately for IBM/FSC the phase out of CFC/ODC solvents, coupled with the implementation of the HCFC solvent, permitted a single cleaning process to remain in effect.

IBM/FSC was able to eliminate Class I ODC solvents and only two major programs required notification of the pending process change. Even then, it was not anticipated that these customers would be strongly opposed to the process changes as any notification to return to the former processes would be an obvious confrontation of two federal agencies dictating to an OEM to disregard the other's requirements. Hence, a period of shady grey exists for an OEM and it's customers, (and regulations). But all can be served when the OEM commences with a good faith effort to resolve the problem, opens a line of communication to each and every customer and lastly, generates the requisite reliability data in a timely manner.

Finally, in keeping with a good faith effort IBM/FSC has publically announced it's approach to ODC elimination, showed data, discussed openly it's problems and concerns with other OEMs and is formally preparing the final data package. Once all data is in place and the processes have been changed without problems, then the customers will be formally notified of the conclusion of the effort. And, at that time, they will be advised that the reliability data and yield data are available for their review upon request. In this manner, IBM/FSC will be able to assure it's contracts administrators that the data has been supplied, "upon request" to the proper authorities within the customer's organmization, all in accordance with MIL-STD-470.

CLEANED LS/NC FLUXES ON HIGH RELIABILITY HARDWARE
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FOOTNOTES

1. IPC-TR-580, Cleaning and Cleanliness Test Program.

2. Tim Crawford: Circuits Assembly, September 1992.

3. Dr. William Kenyon: IPC National Clean/No Clean Soldering Conference Proceedings, November 15-16, 1993.

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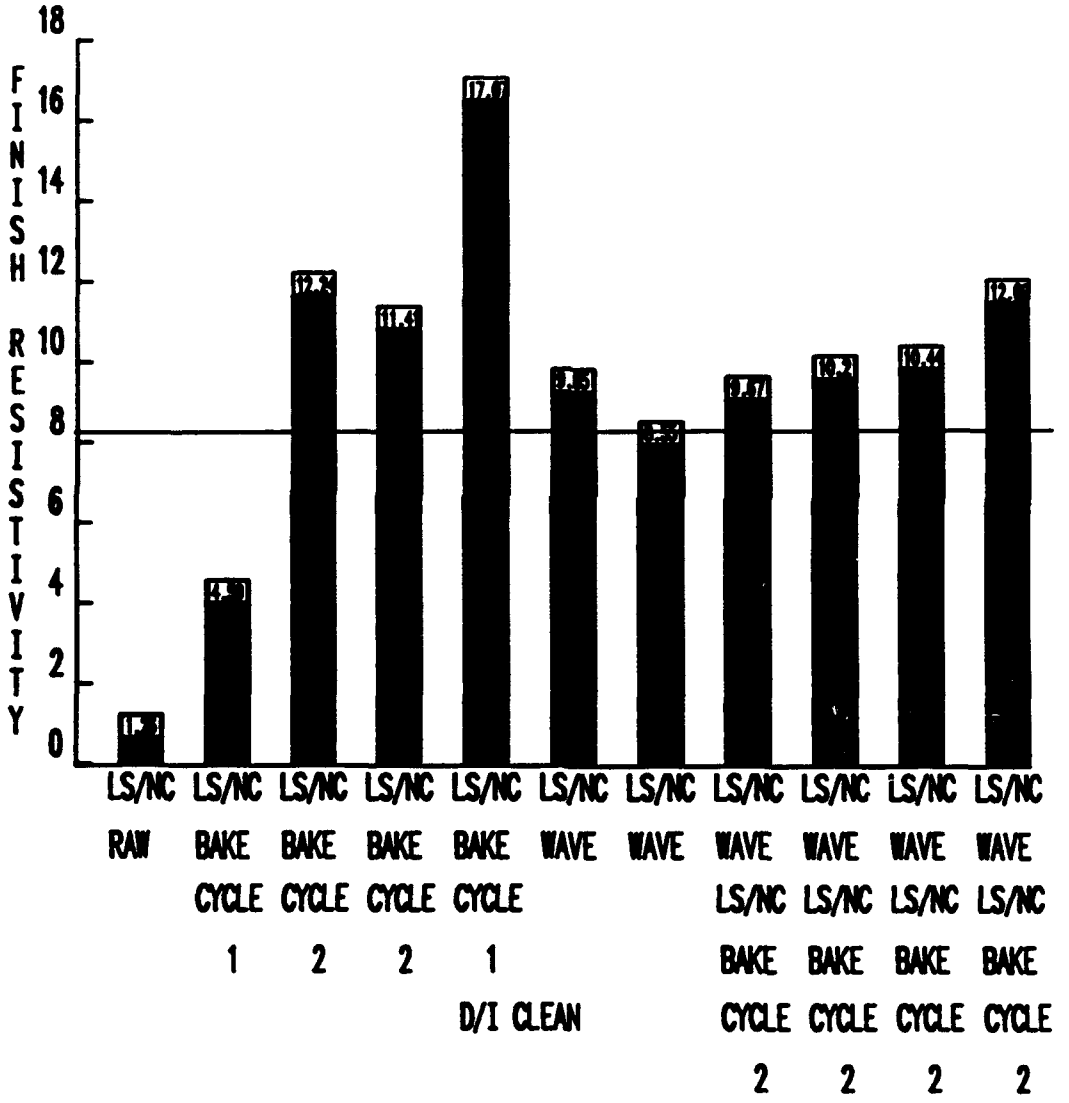

Figure 1. Ionic contamination test results.

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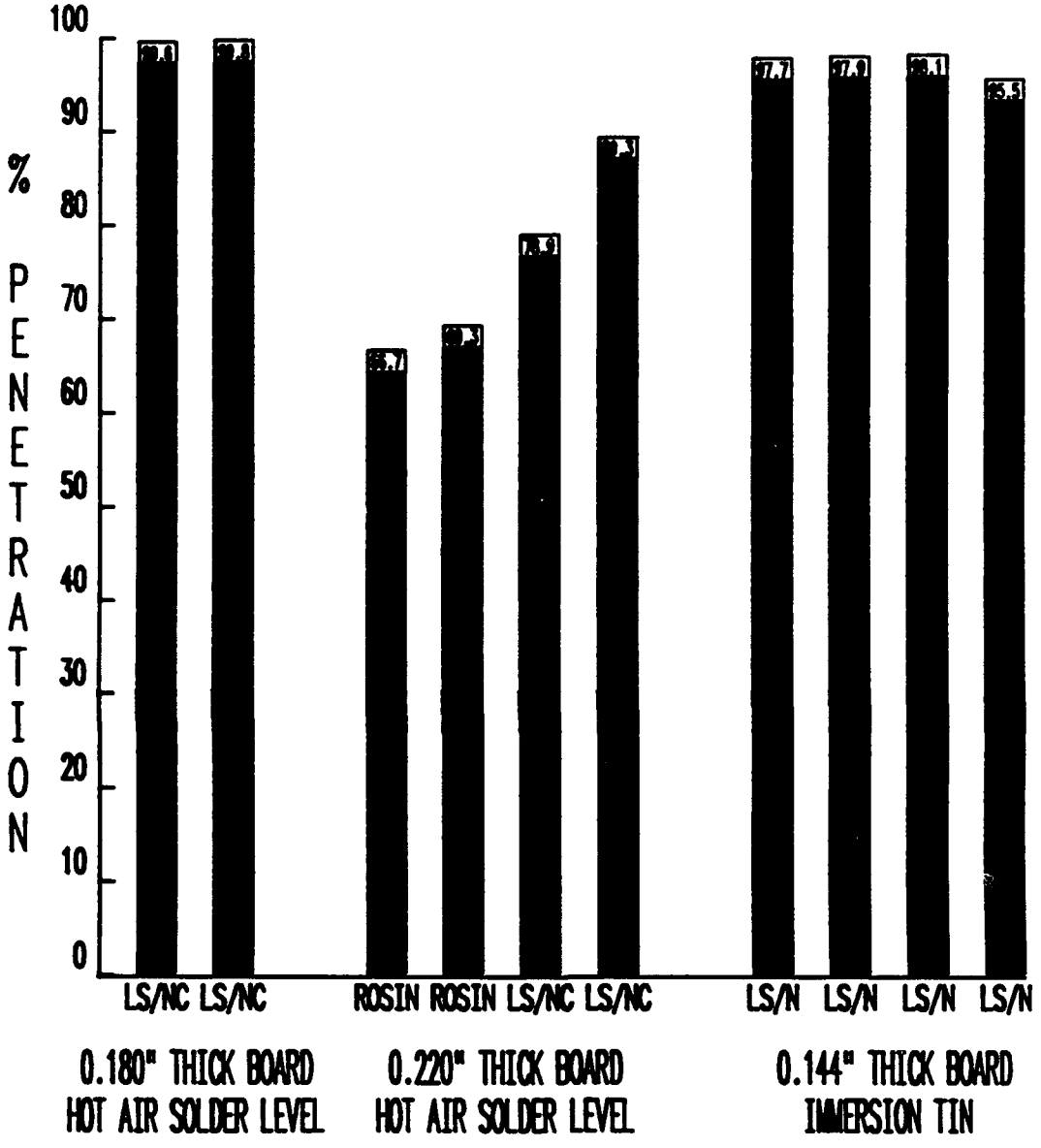

Figure 2. Solder penetration for various assemblies.

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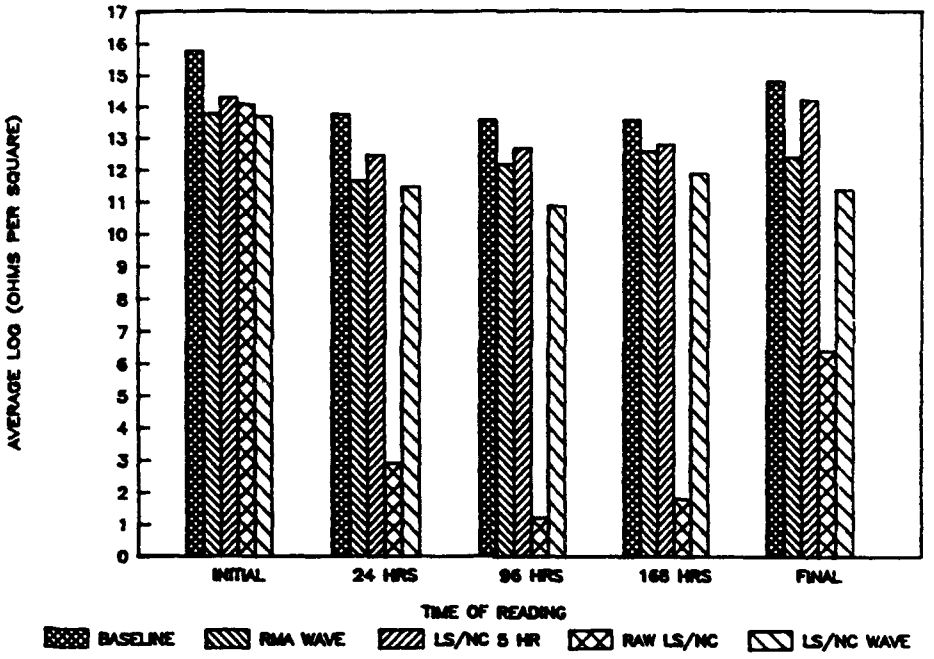

Figure 3. Surface insulation resistance of polyimide boards.

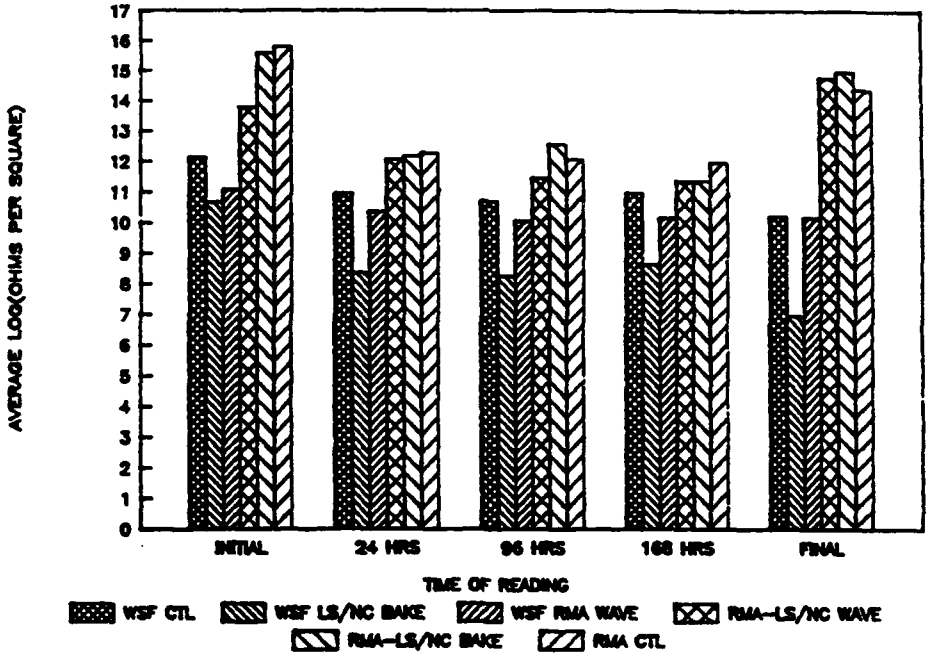

Figure 4. Surface insulation resistance of epoxy boards.

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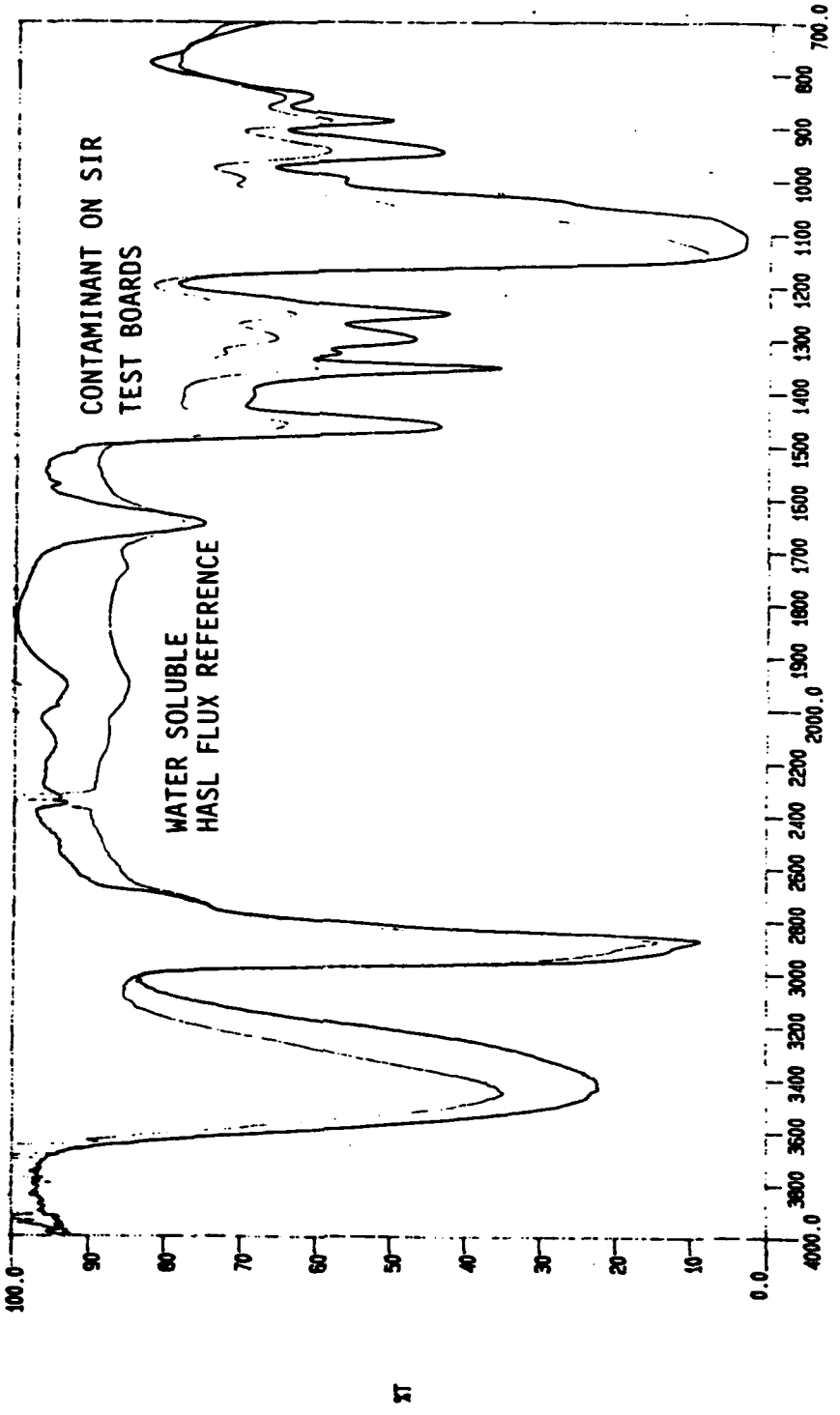

Figure 5. Fourier Transform Infra Red Spectra of contaminant visible following SIR test and water soluble HASL flux reference.

CLEANED LS/NC FLUXES ON HIGH RELIABILITY HARDWARE
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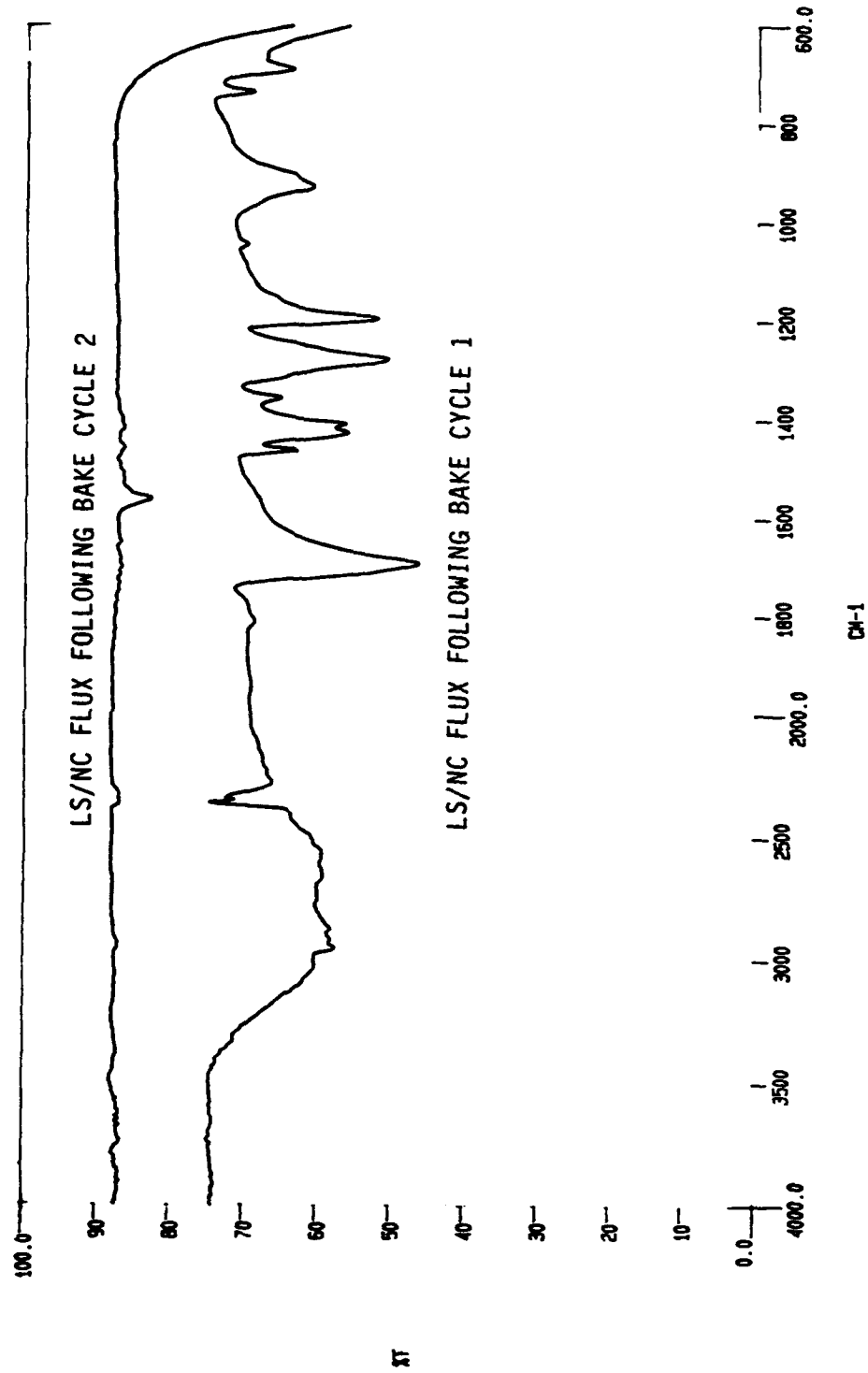


Figure 6. Fourier Transform Infra Red Spectra of LS/NC flux following bake cycle 1 and bake cycle 2.

Patrick M. Scott is Staff Engineer/SMT Process Engineering at IBM/FSC, Owego, New York. He has had 8 years of experience in cleaning, soldering, and various bonding and coating processes. He holds a B.S. degree in Chemical Engineering from Youngstown State University and an M.S. degree in Chemical Engineering from Clarkson University.

Address: Process and Materials Engineering
IBM/FSC
1801 Route 17C
Owego, NY 13811

WAVE SOLDERING PROCESS IMPROVEMENT USING TAGUCHI DOE

by

N.T. Balakrishnan CQE, CFPIM
Manager Manufacturing Engineering
New Bedford Panoramex Corporation
Upland, California 91786

ABSTRACT

This paper describes an Empirical Modeling Method for improving wave soldering yields in a military electronics manufacturing facility. This approach could also be used in a commercial electronics environment.

Empirical models are suitable for determining relationships between input and output variables in an environment where mathematical modeling is impossible. Mathematical models make over simplifying assumptions to represent real world relationships, they do not have neat solution methodology and are generally difficult to construct and understand.

Empirical models, on the other hand are based on statistical design of experiments methodology and can be used to prove on disprove any hypothesis. These models can also support commonly held theories of bounded rationality such as the PRAGMATIST who believes that "IF SOMETHING WORKS, THEN THE THEORY IS VALID" or an IDEOLOGIST who believes that "IF THEORY IS VALID, THEN IT SHOULD WORK".

Both in the commercial and military electronics industry, production of high quality and reliable printed circuit board assemblies is of utmost importance. Wave soldering is the most common method of making solder joint interconnections between electronic devices and the circuit board substrate. It is a process suited for mass manufacturing methodology. High volume repetitive manufacturing often requires processes that can produce near perfect yields at defect rates of 100 to 3,000 parts per million (ppm). Manufacturing practices in industry range from producers achieving as low as 100 ppm defect rates to as high as 30,000 ppm defect rates in wave soldering. High defect rates cause high rework and life cycle costs and creates loss of quality to society in general. Reliable estimates put this at 5 to 10 percent of total gross product value.

There are many approaches to improving yields in the wave soldering process-many involve equipment with better controls to monitor process variables; however, for each printed circuit board these variables need to be determined prior to soldering using empirical modeling methods.

The Full Factorial Design of Experiments Methodology permits the analysis of varying more than one variable at a time and its impact on the output variable.

In a manufacturing environment, where lot sizes are low and unit costs are high, it may not be economical to do Full Factorial Experiments. For example, a design for 5 factors each at 2 levels would need 25 or 32 experiments. In such cases fractional factorial designs using Taguchi's Orthogonal Arrays are more suitable. For a 5 factor design, only 8 experiments are needed using the L8 orthogonal array.

This research paper focuses on determination of process variables that result in ROBUST process design. The process variables chosen for the study include circuit board preheat temperature, conveyors feed, circuit board immersion depth, composition and specific gravity of flux and wave dwell time.

The output of the experiment was the total defect rate per board. Major defects included insufficient solder, peaks, poor wetting, dull/graying solder, blow holes/ voids, excessive solder, solder skips and disturbed solder.

Each variable (factor) was tested at two levels using the L8 orthogonal array used in the fractional factorial experiment.

Several noise factors like age of the circuit board, ambient temperature and humidity were also incorporated in the study.

From the analysis of main effects and interaction effects, the contribution of each factor was determined using the standard ANOVA table.

This helped in the selection of optimal values of the factors which was confirmed by several confirmation runs.

At the conclusion of the experiment, average number of defects was reduced by over 70%.

Introduction:

Wave soldering is as much an art as science. The scientific basis for the wave soldering process is well documented and there are general quidelines for both the design of the circuit board and the soldering process. However general guidelines by themselves cannot be used for the soldering process - the process has to be specifically engineered to suit the given design of the circuit board in order to get optimum results. The process engineering task determines the critical process variables and their values and the end result is characterized by absence of defects or by reduction of defects.

Processes by their very nature tend to drift, tend not to produce repeatable results and also exhibit a high degree of variability. A well engineered process has well defined set of variables and is both repeatable and shows very low levels of variability. Such processes are robust in nature and can be engineered by a combination of scientific guidelines and empirical experimentation. Robust processes are a prerequisite to good product - quality.

Process - Product Quality Dependency

Product quality is a characteristic that describes product performance relative to customer requirements and expectations. Processes with consistent low defect - rates (high yields) will result in product quality with minimal inspection effort. A contemporary view of what constitutes quality is "Conformance to specifications; and as long as specifications are met, there is no need to improve quality". However this view of quality is being supplanted by a more rigorous definition used by a growing community of World Class Manufacturers (WCMs). This definition recognizes the customer's desire to have products that are consistent and are very close to the nominal specification. Any deviation (even within the specification tolerance) from the nominal is by this definition undesirable and will affect the product performance in the long run.

Controlling Variation by Experimentation

In order to produce products that are uniform, variations in process outcomes need to be minimized. Such an approach seeks to identify major variables (parameters) that cause these variations. Once the variables are identified, then their optimum values can be determined by using efficient methods of experimentation. In statistical experimentation variables are also called as factors.

Engineers and scientists typically run tests using combinations of variables (factor values), observe process performance, then modify the values of variables (factors) and rerun the tests. Such an approach may not lead to the correct solution if the test strategies are not properly set-up.

Test strategies like varying one factor at a time holding all the other variables constant, leave out important interaction effects of one factor with one or more factors. The one factor approach also does not use the data in an efficient manner.

On the other extreme, by changing several factors all at the same time; the contributions of each of the factors cannot be determined independently of one another. Some factors may make positive contributions which may be masked by the effects of other factors leading to incorrect conclusions about factor effects.

A scientifically run experiment should utilize all the data and evaluate the effects of factors independently of one another and also predict the main effects of factors and the interaction effects of one or more factors. This is possible by the use of full factorial and fractional factorial experiments. A detailed discussion of the principles is beyond the scope of this paper. References 2 and 3 at the end of this paper deal with the subject matter of experimental design.

A full factorial experiment is practicable when the number of factors (variables) is few and only 2 levels need to be tested. The general expression for the number of trials for a full factorial
experiment with n factors each at 2 levels is 2^n . We can see that the number of trials is fairly high (32) even for n = 5. Most process experiments have at least 5 factors that need to be tested at 2 levels and if the total production quantity is small then it may not be economical to run 32 trials. The time and financial constraints may preclude the use of the full factorial experiments. Other efficient test strategies use partial factorial or fractional factorial experiments.

Taguchi invented the concept of orthogonal arrays to do just this and for every experiment there is a unique orthogonal array that can be used to conduct testing, it the number of factors and levels are known in advance.

The experimenter should be very familiar with the process environment and be able to diagnose the major factors and the factor levels that is intended to be studied, prior to conducting the experiment.

Wave Soldering Process

The wave soldering operation user a Hollis type 24" conveyorized wave soldering machine with two top preheaters and one bottom preheater. All boards are prebaked in an oven at 185°F for at least 1 hour, immediately prior to wave soldering. The foam fluxer uses a pumice stone with a stiff brush that foams the flux.

The flux used is a low solids RMA type 2 flux and the soldering process is in accordance with MIL-STD-2000 requirements. Typically the preheaters are set to preheat the board to 200°F to 215°F in order to activate the flux. The conveyor speed is set between 2.5 feet per minute and 3.7 feet per minute. The appropriate speed is a function of the board dwell time on the wave. Dwell time cannot exceed 5 seconds in a MIL-STD-2000 environment. The board incident angle is set at 7° as it goes over the wave. Wave height is adjusted such that the board immersion depth is between 50% and 75% of the board thickness.

As can be readily seen the scientifically recommended process variable (factor) settings have a wide band width, which needs to be narrowed down to more precise values using empirical experimentation. In order to set-up a meaningful number of trials with different process parameter (factor) settings the experimenter needs to know enough about the process environment and the primacy of each variable that needs to be controlled.

Diagnosing the Process Environment - Wave Soldering

This phase of experimentation is all important and sets the stage for the number of experiments. The determination of which variables (factors) to investigate depends on process knowledge. Since no one single individual has all the knowledge pertaining to the wave soldering process, a good place to start would be to do one or all of the following: i) Brainstorming, ii) Flow Charting, iii) Cause - Effect Diagrams.

Brainstorming is an activity that brings together all stakeholders and soliciting their advice as to what factors to investigate. These could be the Manufacturing Engineer, Process Operator, Quality Engineer, etc.

Flow charting is a formal method of identifying the sequence of steps to be followed and the variables relating to each step. Here the

Manufacturing Engineer or Process Engineer uses accumulated process data to identify appropriate factors and their levels.

Cause and Effect diagram construction begins with the basic effect that is produced and the most probable cause for the effect. The identification of the cause(s) will determine the factors (variables) needed to be experimented.

Cause and Effect diagrams can also be the final product of Brainstorming and Flow charting activity. In general initial investigation should consider as many factors at as few levels as possible in order to have a wider range of options to play with. Also at this stage some factors may not have more than one recommended level which reduces the factor to a constant.

A preliminary search of factors and their effects was done as shown in Table A. Note that the factors are the "most probable cause" for the effect mentioned. A screening of these factors was done to reduce them to a set of manageable factors as shown in Table B. Initially these factors were planned for experimentation at 2 levels as shown in Table B. The result of extensive brain storming and flow charting produced the Cause - Effect diagram shown in Figure 1.

As can be seen, many factors are design related factors which have to be addressed during the printed circuit board fabrication phase, if these are not attended to properly, the opportunity for improved yields in manufacturing are lost forever.

The preliminary Factors - Effects information is a generalized table for the wave soldering process. Most of the effects can be cross
referenced to the MIL-STD-2000A defect code list (including the supplement). Table C shows the MIL-STD-2000A defects codes as currently defined.

The process of screening of Factors to manageable levels was done with a view to reduce the number and variety of factors that can be varied to optimize the process.

In most statistical experiments, sophisticated screening designs like the Plackett - Burman Designs are available - these are useful when not much is known about process variables. In the wave soldering experiment there was sufficient accumulated knowledge to identify the more critical factors from the less critical factors. Also the product was already in production, making it uneconomical to make (in the short run) design/changes to accommodate factors that are defined during these stages. However the designers were aware of most of these factors (like hole to lead ratios, balanced use of ground planes and proper component - lead spacings and orientation) and that these factors were already designed into the system.

Similarly in the fabrication area, the fabrication vendors had to comply with the requirement of MIL-P-5510 which specified levels of acceptance of conditions such as board oxidation, misregistration of mask, board warpage and hole roughness. Proper packaging and storage precautions reduced the moisture problem in the laminate.

In a similar fashion all causes leading to wave soldering defects -arising out of assembly causes were eliminated by proper process engineering methods. Finally the factors within the wave soldering process were investigated for best settings and all but four were assigned preset-values as follows:

FACTORS ELIMINATED	BEST SETTING & RATIONALE
Solder Temperature	500°F based on MIL-STD-2000A Requirements.
Solder Wave Unevenness	The wave profile was kept free of turbulence by periodic preventive maintenance.
Solder Contamination	Solder composition analysis was done every 30 operating cycles (per MIL-STD-2000A requirements) and corrective actions taken.
Flux Specific Gravity, Flux Not Active, Flux Contaminated	Fluxing sub-system and pumice stone were cleaned and kept soaked in solvent after each run.
Conveyor Vibration	Was eliminated by periodic preventive maintenance.
Conveyor Incident Angle	Was preset at 7°F to the horizontal plane.
Board Not Seated Right	Was eliminated by correct fixturing.

Thus only factors that remained to be experimented were:

1. Solder wave height (board immersion depth)
2. Preheater temperature
3 Conveyor speed

To this list was added an additional factor called "Solids Content of Flux", which was thought to play a major role in defect reduction.

Experimental Set-up

Having identified 4 factors at 2 levels, a full factorial experimentation would require 2^4 or 16 experiments. On the other hand use of fractional factorial experiments would reduce the number of experiments or trials. Taguchi (3) has developed a family of fractional factorial matrices which can be utilized in various situations. These are called orthogonal arrays (OAs). For 4 factors, the smallest orthogonal array (OAs) is an L8 (OA) shown in Table D. Each column represents a factor by itself and or a combination of factors indicating interaction effects among factors.

An L8 OA can handle 3 factors at 2 levels and behave like a full factorial experiment with a resolution power of 4. This is equivalent to saying that all main effects (A,B,C) and all interaction effects of second order (AB,AC,BC) and the third order interaction effect (ABC) can all be estimated.

If 4 factors at 2 levels need to be investigated in the experiment, then a full factorial experiment requires 2^4 or 16 trials. If the lot size is small and it's possible to run only 8 trials, an L8 OA can be used in a fractional factorial experiment. However the resolution power of this experiment drops to 2. This means that all main effects (A,B,C,D) can be estimated but the interaction effect of second order are confounded (mixed) with each other.

From the standpoint of the experimenter, some interactions cannot be studied. This may not cause any serious problems if it is known in advance which second order interaction effect are strong and which are weak. In the present case of wave soldering experiment, based on past experience the main effects of factors A, B, C, D and the interaction effects of BxC, BxD and CxD were the only ones that were considered significant.

The experiment could have been made Robust by modifying the L8 OA, by including 3 external noise factors - one the age of the circuit board (level 1 it less than 3 months, level 2 it greater than 3 months) and the second the ambient relative humidity (level 1 for relative humidity less than 40%, level 2 for relative humidity greater than 40%) and the third the ambient temperature (level 1 for temperature less than 75°F, level 2 for temperature greater than 75°F).

The noise factors would have introduced an outer array using the L4 OA (Table D). However the small lot size did not permit more than one replication for each trial.

The order of trials included a complete randomization using standard random number tables. This was done with a view to make the trials unbiased for any unknown and

uncontrollable factors that may have varied during the entire experiment.

Results and Conclusions

The computation of the ANOVA Tables for the various trial runs showed that the optimum results were obtained for the following factor values.

Factor	Level
Specific Gravity/ Solids % of Flux (A)	0.875 / 30%
Circuit Card Preheat Temperature (B)	210°F
Circuit Card Immersion Depth (C)	70% Thickness
Conveyor Speed (D)	3.5 Feet per Minute

The graphs for the main effects and interaction effects are shown in Figure 2. As can be seen, the main effects and interaction effects were both predominant.

FIGURE 1

SOLDER JOINT DEFECTS, CAUSE - EFFECT DIAGRAM

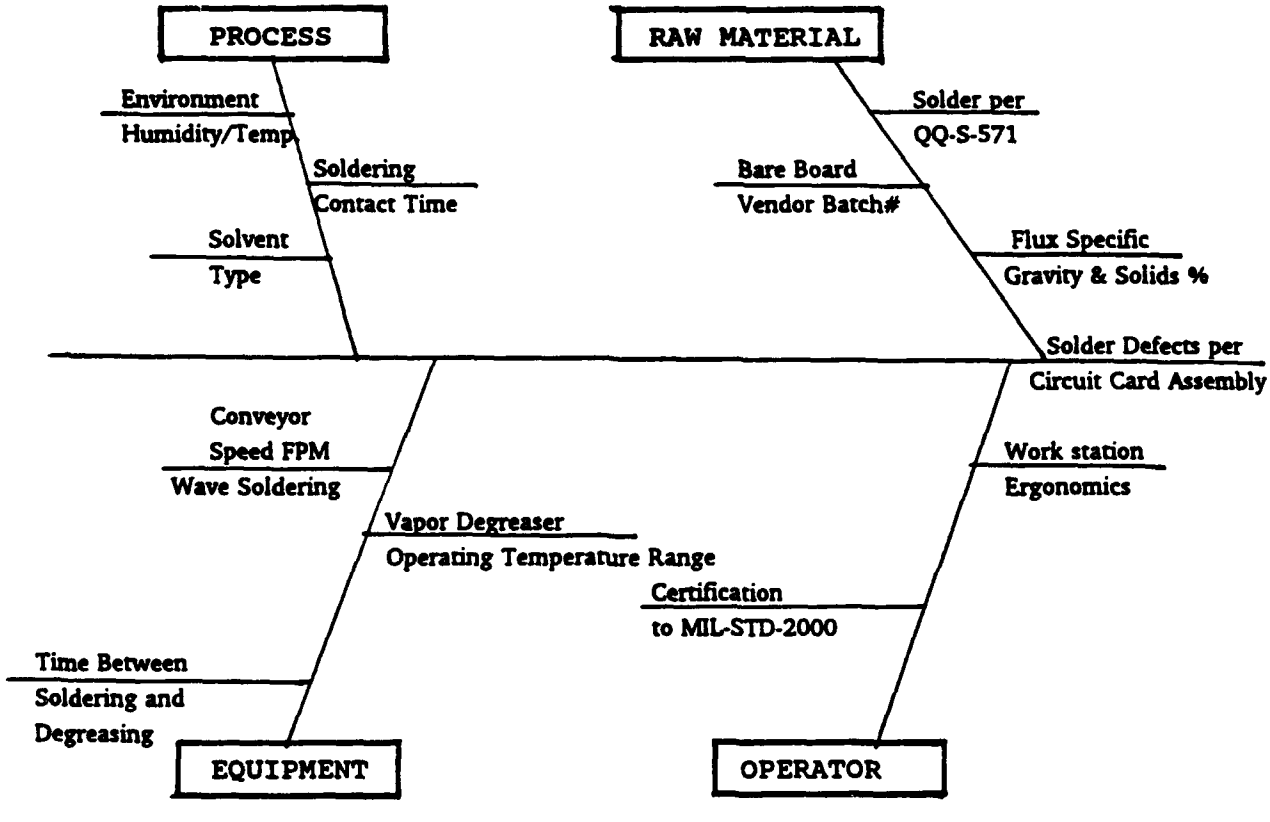


TABLE B

Set of Manageable Factors

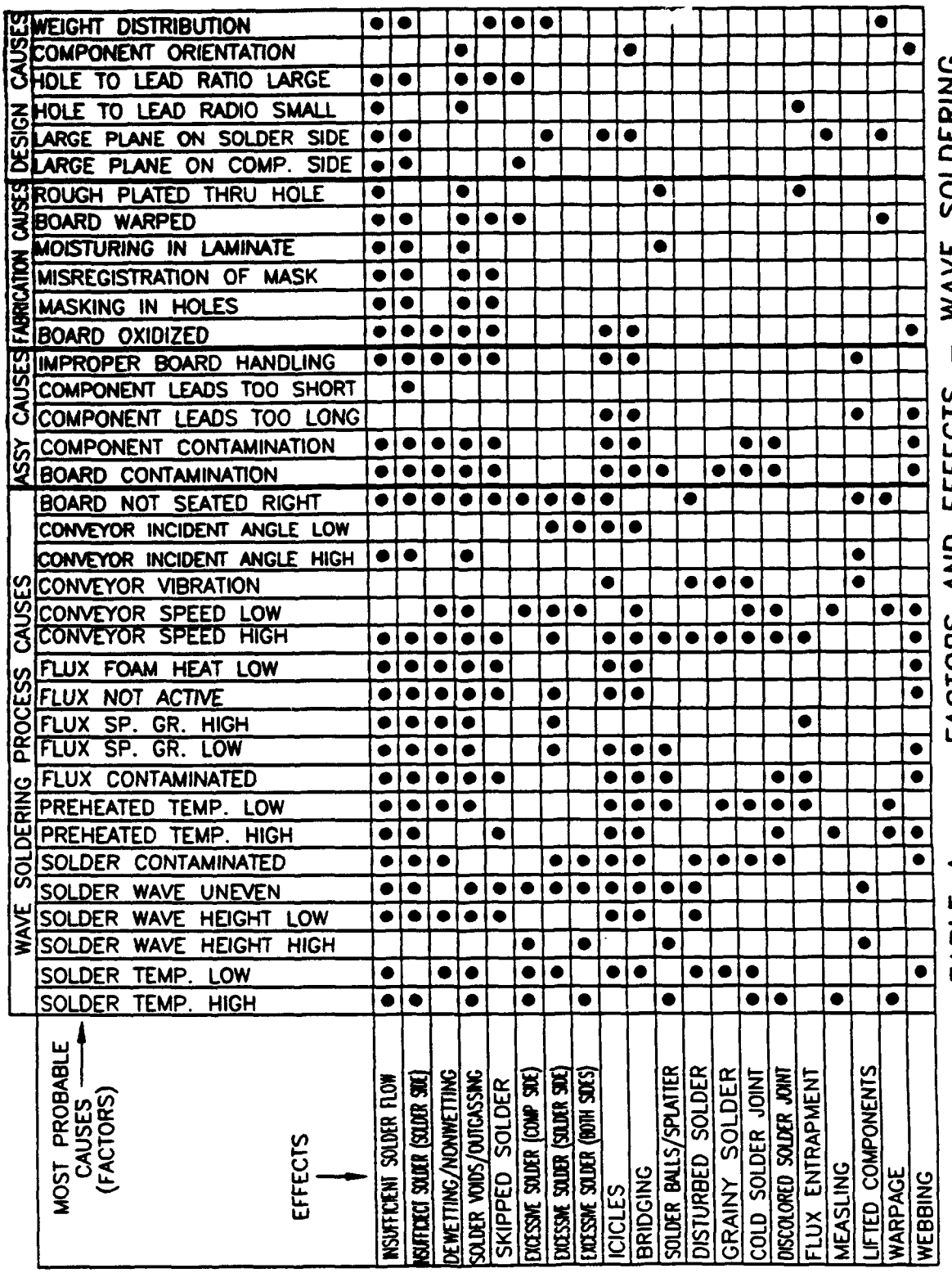
Factors	Symbol	Level 1	Level 2
Specific Gravity/Solids % of Flux	A	0.875 15%	0.875 30%
Circuit Card Preheat Temperature	B	190°F	210°F
Circuit Card Immersion Depth Thickness of in Solder Wave Circuit Card	C	50% of Thickness of Circuit Card	70% of
Conveyor Speed Ft/Min.	D	2.5 Ft/Min.	3.5

TABLE C

MIL-STD-2000A DEFECT LIST (SOLDERING)

- Charred printed wiring board.
- Movement between conductors, excessive solder, bridging.
- Flux residue, foreign material.
- Fractured, cracked or disturbed solder connections.
- More than 10% of the periphery of the solder connection non wetted or dewetted.
- Lifted lands or conductors separated by more than the thickness (height) of the conductor.
- Delaminated or blistered printed wiring base material.
- Voids or blowholes in conjunction with the minimum allowable solder volume. This applies to all types of solder connections.
- Plated through holes with or without leads with more than 25% recession of the solder.
- Unsoldered connections.
- Component not sufficiently supported.
- Excessive solder with lead not discernable.
- Overheated solder.
- Excessive warp or twist after soldering.

(NOTE: Defects arising out of improper assembly process, or design have been omitted)

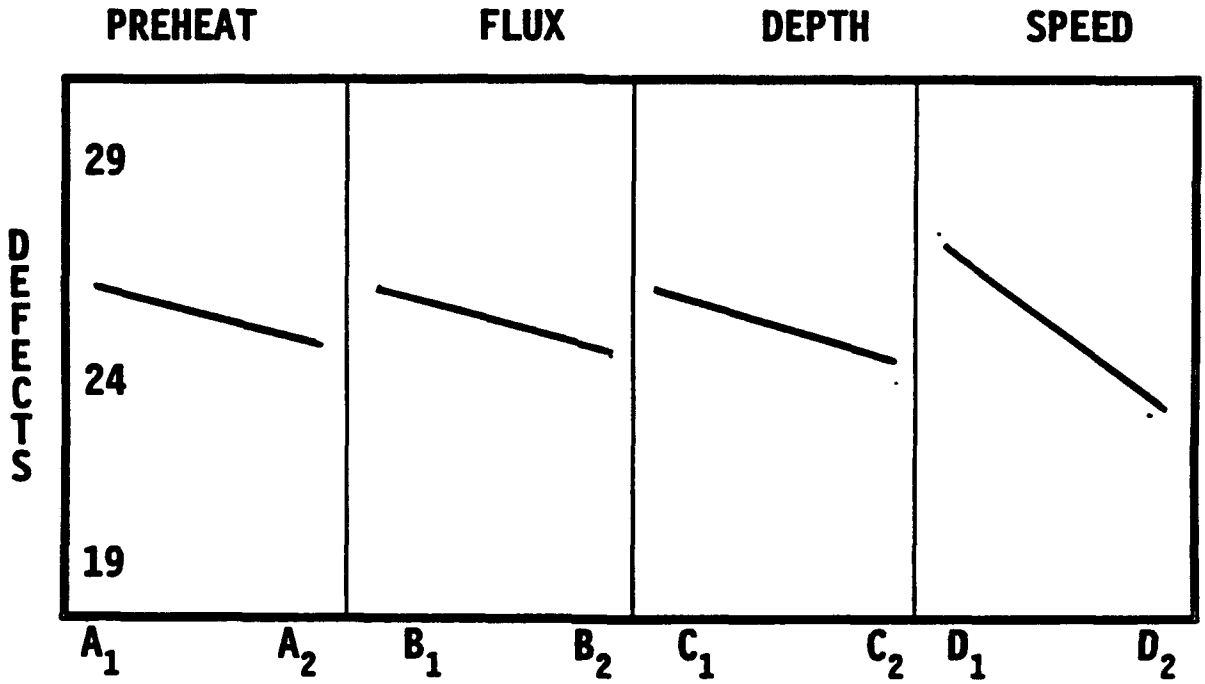


MOST PROBABLE CAUSES (FACTORS) ↑ / EFFECTS →	INSUFFICIENT SOLDER FLOW	INSUFFICIENT SOLDER (SOLDER SIDE)	DEWETTING/NONWETTING	SOLDER VOIDS/OUTGASSING	SKIPPED SOLDER	EXCESSIVE SOLDER (COMP SIDE)	EXCESSIVE SOLDER (SOLDER SIDE)	EXCESSIVE SOLDER (BOTH SIDES)	ICICLES	BRIDGING	SOLDER BALLS/SPLATTER	DISTURBED SOLDER	GRAINY SOLDER	COLD SOLDER JOINT	DISCOLORED SOLDER JOINT	FLUX ENTRAPMENT	MEASLING	LIFTED COMPONENTS	WARPAGE	WEBBING
WAVE SOLDERING PROCESS CAUSES: SOLDER TEMP. HIGH	●	●		●		●		●			●			●	●		●			
SOLDER TEMP. LOW	●		●	●		●			●	●		●	●	●						●
SOLDER WAVE HEIGHT HIGH						●		●			●							●		
SOLDER WAVE HEIGHT LOW	●	●	●	●	●				●	●		●							●	
SOLDER WAVE UNEVEN	●	●		●	●	●	●	●	●	●	●	●						●		
SOLDER CONTAMINATED	●	●	●				●	●	●	●		●	●	●	●				●	●
PREHEATED TEMP. HIGH	●	●			●				●	●					●		●		●	●
PREHEATED TEMP. LOW	●	●	●	●					●	●	●		●	●	●	●			●	●
FLUX CONTAMINATED	●	●	●	●	●				●	●	●				●	●				●
FLUX SP. GR. LOW	●	●	●	●			●		●	●	●									●
FLUX SP. GR. HIGH	●	●	●	●			●									●				
FLUX NOT ACTIVE	●	●	●	●	●		●			●										●
FLUX FOAM HEAT LOW	●	●	●	●	●					●										●
CONVEYOR SPEED HIGH	●	●	●	●	●		●			●	●	●	●	●	●	●				●
CONVEYOR SPEED LOW			●	●		●	●	●		●				●	●		●			●
CONVEYOR VIBRATION												●	●	●				●		
CONVEYOR INCIDENT ANGLE HIGH	●	●		●														●		
CONVEYOR INCIDENT ANGLE LOW							●	●	●	●										
BOARD NOT SEATED RIGHT	●	●	●	●	●	●	●	●	●			●						●	●	
ASSY CAUSES: BOARD CONTAMINATION	●	●	●	●	●				●	●	●		●	●	●					●
COMPONENT CONTAMINATION	●	●	●	●	●				●	●				●	●					●
COMPONENT LEADS TOO LONG									●	●								●		●
COMPONENT LEADS TOO SHORT		●																●		
IMPROPER BOARD HANDLING	●	●	●	●	●				●	●								●		
FABRICATION CAUSES: BOARD OXIDIZED	●	●	●	●	●				●	●										●
MASKING IN HOLES	●	●		●	●															
MISREGISTRATION OF MASK	●	●		●	●															
MOISTURING IN LAMINATE	●	●		●							●									
BOARD WARPED	●	●		●	●	●													●	
ROUGH PLATED THRU HOLE	●			●							●									
DESIGN CAUSES: LARGE PLANE ON COMP. SIDE	●	●				●														
LARGE PLANE ON SOLDER SIDE	●	●					●		●	●							●		●	
HOLE TO LEAD RADIO SMALL	●			●														●		
HOLE TO LEAD RATIO LARGE	●	●		●	●	●														
COMPONENT ORIENTATION				●						●										●
WEIGHT DISTRIBUTION	●	●			●	●	●												●	

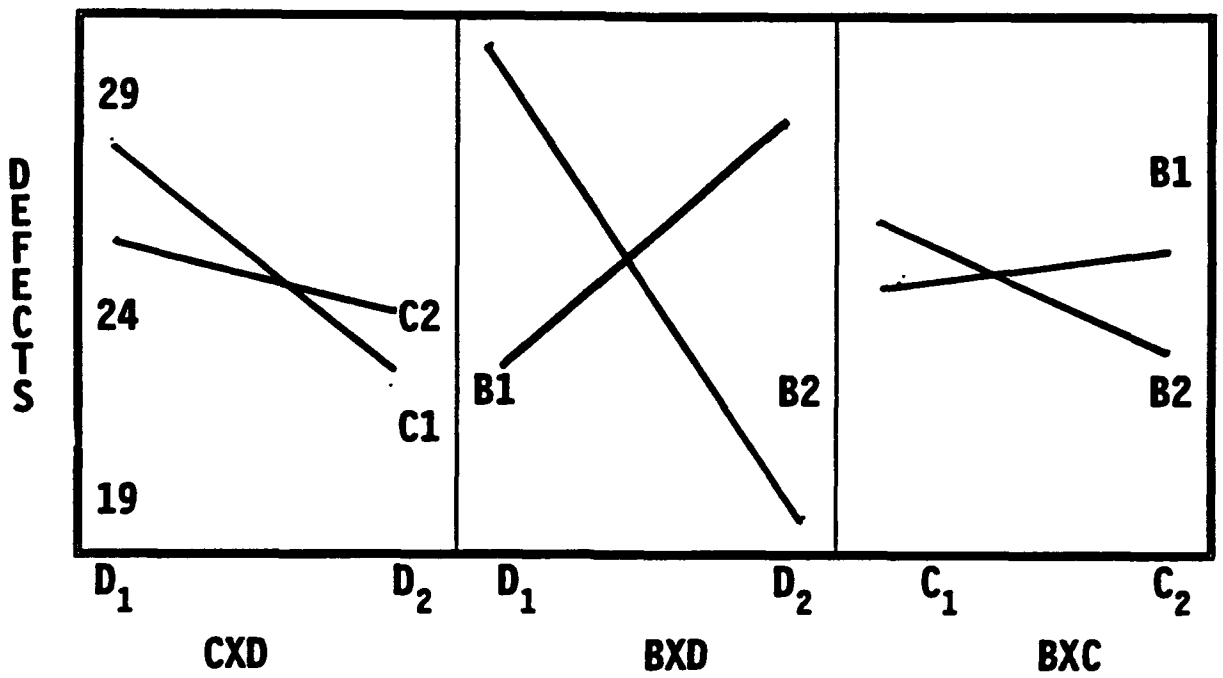
TABLE A FACTORS AND EFFECTS – WAVE SOLDERING

FIGURE 2

MAIN EFFECTS



INTERACTION EFFECTS



								L4 OA outer array (noise factors)			
								Z	1	2	2	1
								Y	1	2	1	2
								X	1	1	2	2
	L8 OA inner array (control factors)							ONE RESPONSE ONLY			
	A	*B*	*C×D*	*C*	*B×D*	*B×C*	*D*				
	Column no.							Data			
Trial no.	1	2	3	4	5	6	7	y_1	y_2	y_3	y_4
1	1	1	1	1	1	1	1	24	•	•	•
2	1	1	1	2	2	2	2	30	•	•	•
3	1	2	2	1	1	2	2	20	•	•	•
4	1	2	2	2	2	1	1	28	•	•	•
5	2	1	2	1	2	1	2	26	•	•	•
6	2	1	2	2	1	2	1	22	•	•	•
7	2	2	1	1	2	2	1	32	•	•	•
8	2	2	1	2	1	1	2	18	•	•	•

Table D Experimental Results.

N. T. "Bala" Balakrishnan is Manager, Manufacturing Engineering, at New Bedford Panoramex Corporation, Upland, California. He has had 18 years of experience in operations and manufacturing management in commercial and military electronics management, and is a member of the adjunct faculty, California State Polytechnic University, Pomona, California.

He is a Certified Quality Engineer of the American Society for Quality Control and is certified at the Fellow level of CFPIM, American Production, Inventory Control Society. He is also a member of the Quality Progress Editorial Board of the American Society for Quality Control.

Bala received his BSME degree from the Indian Institute of Technology, Bombay, India, and his MSIE degree from the Indian Institute of Technology, Kharaqpur, India. He earned an MBA degree from the John Anderson Graduate School of Management of the University of California at Los Angeles.

Address: New Bedford Panoramex Corporation
1037 W. Ninth Street
Upland, California 91786

LONG-TERM RELIABILITY REQUIREMENTS AND THEIR ASSURANCE FOR SURFACE MOUNT SOLDER JOINTS FOR U.S. AIR FORCE (AVIP) AVIONICS

by

Werner Engelmaier
Engelmaier Associates, Inc.
Mendham, NJ 07945
(201)543-2747

ABSTRACT

The reliability of electronic systems depends in no small measure on the long-term reliability of the surface mount solder attachments of electronic components within the system. Thus, surface mount solder attachment requires that explicit design attention is provided to assure long-term reliability given the requirements of the application. Many applications, such as automotive electronics and military avionics applications operate under highly variable and complex thermal loading conditions. Under the AVIP (Avionics Integrity Program) of the U.S. Air Force a 20-year service life of 8,000 flight and 4,000 maintenance hours is required, which is to be simulated with 59 different loading conditions for the F-22 'Stealth' fighter.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches, and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches.

The different loading conditions in combination with the design parameters of the assembly result in different cyclic damage. This damage is cumulative and needs to be considered in the assessment of the reliability of the system. In addition, each solder attachment of each component in the system contributes to the threat to the reliability of the system.

In this paper the assessment of the contributed fatigue damage of each loading condition to the total cumulative fatigue damage will be discussed. Further, a method to evaluate the system reliability given a multiplicity of equal and different components will be shown.

INTRODUCTION

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal, and electrical interfaces (or

attachments) between these elements. One of these interface types, surface mount solder attachments, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed wiring board and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed wiring board. The characteristics of these three elements together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

TABLE 1. Realistic Representative Use Environments, Service Lives, And Acceptable Cumulative Failure Probabilities For Surface Mounted Electronics By Use Categories [Reference 7].

USE CATEGORY	WORST-CASE USE ENVIRONMENT					Years of Service	Acceptable Failure Risk, %
	Tmin °C	*Tmax* °C	ΔT (1) °C	t_D hrs	Cycles/ year		
1 CONSUMER	0	+60	35	12	365	1-3	~1
2 COMPUTERS	+15	+60	20	2	1460	~5	~0.1
3 TELECOMM	-40	+85	35	12	365	7-20	~0.01
4 COMMERCIAL AIRCRAFT	-55	+95	20	12	365	~20	~0.001
5 INDUSTRIAL& AUTOMOTIVE -PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
6 MILITARY GROUND&SHIP	-55	+95	40 &60	12 12	100 265	~5	~0.1
7 SPACE leo	-40	+85	35	1	8760	5-20	~0.001
7 SPACE geo				12	365		
8 MILITARY AVIONICS a	-55	+95	40	2	365	~10	~0.01
8 MILITARY AVIONICS b			60	2	365		
8 MILITARY AVIONICS c			80	2	365		
			&20	1	365		
9 AUTOMOTIVE -UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition

(1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT_e.

TABLE 2. Avionics Thermal Cyclic Environment For The F-22 Fighter For A 20 Year Service Life, Including Post-Fabrication Stress Screening, Atp, And Storage, As Well As 8,000 Flight Hours And 4,000 Hours During Ground Maintenance Events [Reference 8].

Cyclic Environment Number	Loading Condition	Number of Cycles	Tmin °C	Tmax[1] °C	ΔT °C	Dwell Time min
1	ESS	10	-40	70[2]	110	12
2	ATP	10	25	70	45	12
3	Storage	550	15	37	22	715
4/5		1/ 1	-40	85/70[1][2]	125/110	90
6/7	Flight/	1/ 1	-35	85/70[1][2]	120/105	90
8/9	Maintenance	3/ 1	-30	85/70[1][2]	115/100	90
10/11		7/ 3	-25	85/70[1][2]	110/ 95	90
12/13		13/ 7	-20	85/70[1]	105/ 90	90
14/15		23/ 11	-15	85/70[1]	100/ 85	90
16/17		60/ 30	-10	85/70[1]	95/ 80	90
18/19		196/ 98	-5	85/70[1]	90/ 75	90
20/21		441/221	0	85/70[1]	85/ 70	90
22/23		617/309	5	85/70[1]	80/ 65	90
24/25		737/368	10	85/70[1]	75/ 60	90
26/27		835/417	15	85/70[1]	70/ 55	90
28/29		929/465	20	85/70[1]	65/ 50	90
30/31		849/425	25	85/70[1]	60/ 45	90
32/33		474/237	30	85/70[1]	55/ 40	90
34/35		113/ 57	35	85/70[1]	50/ 35	90
36/37		36/ 18	40	85/70[1]	45/ 30	90
38/39		1/ 1	45	85/70[1]	40/ 25	90
40		1	-50	-47[3]	3	715
41	Non-Flight	1	-45	-36[3]	9	715
42	Days	1	-40	-30[3]	10	715
43		1	-35	-24[3]	11	715
44		1	-30	-19[3]	11	715
45		2	-25	-14[3]	11	715
46		5	-20	-9	11	715
47		9	-15	-4	11	715
48		25	-10	2	12	715
49		83	-5	7	12	715
50		171	0	12	12	715
51		224	5	17	12	715
52		232	10	23	13	715
53		232	15	28	13	715
54		260	20	33	13	715
55		196	25	38	13	715

TABLE 2. (Continued).

Cyclic Environment Number	Loading Condition	Number of Cycles	Tmin °C	Tmax(1) °C	ΔT °C	Dwell Time min
56		42	30	47	17	715
57		2	35	52	17	715
58		1	40	55	15	715
59		1	45	58	13	715
Total Number of Cycles		10,055				

(1) The supplier must determine the peak temperatures for inflight and ground maintenance conditions based on component design and cooling interface conditions.
(2) Conditions violate Creep-Fatigue Caveat 2 on low- to high-temperature cycling.
(3) Conditions violate Creep-Fatigue Caveat 3 on low-temperature cycling.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches [References 1-5], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches [References 4 and 6].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the use environment. In Table 1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated [Reference 7].

However, sometimes these use conditions can be rather complex. In Table 2 the environments that need to be considered in the reliability assessment of the electronics for the new F-22 fighter jet are given [Reference 8]. The avionics thermal spectrum for the F-22 comprises no less than 59 different environments the impact of which on the solder attachment fatigue damage and thus the surface mount attachment reliability need to be considered in the reliability analysis and the 'Design for Reliability' of the F-22 electronic assemblies.

In this paper the procedures necessary to assess the impact of multiple loading conditions as well as of a multiplicity of different components on the reliability of surface mount solder attachments of the system are discussed.

FATIGUE LIFE PREDICTION FOR SOLDER JOINTS

It has been experimentally shown [References 1, 9, and 10] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation [Reference 11] developed for more typical engineering metals. This equation, subject to some caveats listed later, relates the cyclic visco-plastic strain energy [Reference 12], represented by the cyclic fatigue damage term, ΔD, to the mean cyclic fatigue life

$$\overline{N_f} = \frac{1}{2}\left[\frac{2\varepsilon_f'}{\Delta D}\right]^{\frac{1}{c}} \quad (1)$$

where ε_f' = fatigue ductility coefficient, ≈0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of ε_f' is expected to be different).

Solder, uniquely among the commonly used engineering metals, readily creeps and stress-relaxes at normal use temperatures; the rate of creep and stress-relaxation is highly temperature- and stress-level-dependent. Thus, the cyclic fatigue damage term, ΔD, for practical reasons has to be based on the total potential damage at complete creep/stress relaxation of the solder. For cyclic conditions that do not allow sufficient time for complete stress relaxation ΔD is larger than the actual fatigue damage. The temperature- and time-dependent exponent, c, compensates for the incomplete stress relaxation and is given by

$$c = -0.442 - 6\text{x}10^{-4}\overline{T_{SJ}} + 1.74\text{x}10^{-2}\ln\left(1 + \frac{360}{t_D}\right) \quad (2)$$

where $\overline{T_{SJ}}$ is the mean cyclic solder joint temperature and t_D is the half-cycle dwell time in minutes.

While the physical parameters define the mean cyclic fatigue life, solder attachment failures for a group of identical components will follow a distribution—like all fatigue results—which typically is best described by a Weibull statistical distribution [Reference 13]. Thus, the fatigue life at any given failure probability can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable failure probability, x, is given by

$$N_f(x\%) = \overline{N_f}\left[\frac{\ln(1 - 0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \quad (3)$$

The cyclic fatigue damage term for leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength, is

$$\Delta D(leadless) = \left[\frac{FL_D\,\Delta\alpha\,\Delta T_e}{h}\right] \quad (4)$$

For compliant leaded solder attachments, where the solder joint stresses are below the yield strength and thus are not bounded by it, the cyclic fatigue damage term is

$$\Delta D(leaded) = \left[\frac{FK_D\,(L_D\,\Delta\alpha\,\Delta T_e)^2}{(133\text{ psi})Ah}\right] \quad (5)$$

where for metric units the scaling coefficient is 919 kPa instead of 133 psi. Equations 4 and 5 contain the design parameters that have a first-order influence on the reliability of SM solder attachments. They are:

A = effective minimum load bearing solder joint area ,
F = empirical "non-ideal" factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, brittle inter-metallic compounds, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 1 through 5; $1.5>F>1.0$ for column-like leadless solder attachments, $1.2>F>0.7$ for leadless solder attachments with fillets (castellated chip carriers and chip components), $F\approx 1$ for solder attachments utilizing compliant leads;
h = solder joint height, for leaded attachments $h\cong 1/2$ of solder paste stencil depth as a representative dimension for the average solder thickness,
K_D = "diagonal" flexural stiffness of unconstrained, not soldered, component lead, determined by strain energy methods (see References 14, 15, 16 and 17) or finite element analysis,
$2L_D$ = maximum distance between component solder joints measured from component solder joint pad centers,
N = (design life times cyclic frequency), number of operating cycles during product life,
$N_f(x\%)$= number of operating cycles to $x\%$ failure probability,
T_C, T_S = steady-state operating temperature for substrate, component ($T_C>T_S$ for power dissipation in component) during high temperature dwell,
$T_{C,0}$, $T_{S,0}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,0}=T_{S,0}$,
$\overline{T_{SJ}}$ = $(1/4)(T_C+T_S+T_{C,0}+T_{S,0})$, mean cyclic solder joint temperature,
α_C, α_S = coefficient of thermal expansion (CTE) for component, substrate,
β = Weibull shape parameter, slope of Weibull probability plot, typically 4 for stiff leadless attachments and 2 for compliant leaded attachments,
ΔD = potential cyclic fatigue damage at complete stress relaxation,
ΔT_C = $T_C-T_{C,0}$, cyclic temperature swing for component,
ΔT_e = $[(\alpha_S\Delta T_S-\alpha_C\Delta T_C)/\Delta\alpha]$, equivalent cycling temperature swing, accounting for component power dissipation effects as well as component external temperature variations ($\Delta\alpha\neq 0$),
ΔT_S = $T_S-T_{S,0}$, cycling temperature swing for substrate (at component),
$\Delta\alpha$ = $|\alpha_C-\alpha_S|$, absolute difference in thermal expansion coefficients component and substrate, CTE-mismatch.

CAVEAT 1 — SOLDER JOINT QUALITY

The solder joint fatigue behavior and the resulting reliability prediction relationships, Eqs. 1 through 5, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the intermetallic compound (IMC) layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the 'weakest link' in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to

the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing proper metallurgical bond of the solder to the underlying metal; brittle intermetallic compound layers too thick due to too many or improperly long high temperature processing steps.

CAVEAT 2 — LARGE TEMPERATURE EXCURSIONS

Solder joints seeing large temperature swings which extend significantly both below and above the temperature region from -20 to +20°C in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in Eq. 1 [Reference 18]. The damage mechanism is different than for more typical use conditions and is likely dependent on overstress and recrystallisation considerations.

CAVEAT 3 — HIGH FREQUENCY/LOW TEMPERATURES

For high-frequency applications, $f > 0.5$ Hz or $t_D < 1$ sec, e.g., vibration, and/or low temperature applications, $T_C < 0°C$, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson [Reference 8] fatigue relationship might be more appropriate. This relationship is

$$N_f = \frac{1}{2}\left[\frac{2\varepsilon_f'}{\Delta\gamma_p}\right]^{\frac{1}{c}} \tag{6}$$

where
$\Delta\gamma_p$ = cyclic plastic strain range,
c = ≈–0.6,
β = ≈3.

CAVEAT 4 — LOCAL CTE MISMATCH

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicone-on-silicone (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations 4 and 5 do not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an inter-facial stress analysis [Reference 19] and appropriate accelerated testing.

For leaded surface mount components with lead materials that have CTEs significantly lower than copper alloy materials, e.g. Kovar or Alloy 42, the results from Eqs. 1 and 5 will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included.

CAVEAT 5 — VERY STIFF LEADS/LARGE EXPANSION MISMATCHES

Equations 4 and 5 differentiate between surface mount solder attachments that are leadless and those with compliant leads. Leadless solder attachments presume substantial plastic strains due to yielding prior to creep and stress relaxation, whereas compliant leads

prevent stresses in the solder joints to reach levels where substantial yielding can take place.

However, there is an intermediate region that is not covered by these assumptions. For very stiff leads (e.g., SM connector headers), perhaps at lead stiffnesses $K_D > \sim 500$ lb/in (~87.6 N/mm) and/or for very large thermal expansion mismatches (e.g., ceramic multichip modules (MCM) on FR-4) resulting in strain ranges $\Delta\gamma > \sim 10\%$, the damage estimates in Eq. 5 can be substantially in error. In general, caution might be indicated in all instances were the predicted life is less than 1000 cycles.

For very stiff leads the stresses calculated in Eq. 5 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. 5 needs to be bounded by the yield strength in shear.

For very large thermal expansion mismatches the full displacements will not be transmitted to the solder joints; possible exceptions are situations where very stiff leads are present as well in which case the solder joint reliability is best estimated using Eq. 1 for leadless solder attachments. The strain range that can be accommodated by creep and stress relaxation in the solder joints can be significantly exceeded by the displacements resulting from very large thermal expansion mismatches and the cyclic fatigue damage would be significantly overestimated.

RELIABILITY REQUIREMENTS

MULTIPLE CYCLIC LOAD HISTORIES — AVIP

The typical design service life under the Avionics Integrity Program (AVIP) of the U.S. Air Force is given as 20 years with thermal loading cycles similar to those given in Table 2. The initial reliability objective is typically stated as an allowable net cumulative damage ratio (CDR).

Multiple cyclic load histories (see Tables 1 and 2) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative—this assumption underlies Eq. 1 as well—and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [Reference 20] can be applied.

The cumulative damage ratio (CDR) is calculated as the sum of the ratios of the number of occurring load cycles to the average number of load cycles to failure for each load and is

$$\text{CDR} = \sum_{j=1}^{j} \frac{N_j}{N_{fj}} < 1 \qquad (7)$$

where

N_j = actually applied number of cycles at a specific cyclic load level j,
N_{fj} = fatigue life at the same specific cyclic load level j alone.

The fatigue life is frequently not completely specified and is normally taken to be the mean cyclic fatigue life. Equation 7 can be used with the allowable CDR significantly less than unity to provide margins of safety, or more accurately, margins of ignorance.

Because the failure of solder joints results from wearout due to fatigue, the failure rate is continuously increasing. This is in stark contrast to the reliability design philosophy of MIL-HDBK-217 [Reference 21] which presumes a constant failure rate. These increasing failure rates are properly represented by an appropriate statistical failure distribution, which for wearout mechanisms is most often the Weibull distribution. Weibull distributions can and do have significantly different slopes.

Thus, to assure low failure risks, the fatigue life should be specified at the acceptable cumulative failure probability at the end of the design life as per Eq. 3. Thus, Eq. 7 is more appropriately written as

$$\mathrm{CDR}(x\%) = \sum_{j=1}^{j} \frac{N_j}{N_{fj}(x\%)} = 1$$

where
$\mathrm{CDR}(x\%)$ = cumulative damage ratio resulting in a cumulative failure probability of $x\%$,
$N_{fj}(x\%)$ = fatigue life at the cyclic load level j and a failure probability of $x\%$.

This approach works very well for the design of the solder attachment for a single component. However, it does not lend itself well for a reliability analysis of a given design.

SYSTEM RELIABILITY EVALUATION

Equations 1 through 8 address the reliability of the SM solder attachment of individual components. Systems consist of a variety of different components most of which occur in multiple quantities. Further, as shown in Tables 1 and 2, many use environments cannot and should not be represented by a single thermal cyclic environment, and accumulating fatigue damage from other sources, such as cyclic thermal environments as described in Caveats 2 and 3 as well as vibration, needs to be included also.

For a multiplicity of components, i, in the system, the effect of the various components on the system reliability can be determined from

$$F_{\Sigma}(N) = 1 - \exp\left\{\ln(1 - 0.01x)\sum_{i=1}^{i} n_i\left[\sum_{j=1}^{j}\frac{N_{i,j}}{N_{fi,j}(x\%)}\right]^{\beta}\right\} \qquad (9)$$

where
$F_{\Sigma}(N)$ = system cumulative failure probability after N total cycles,

n_i = number of components of type i,
$N_{i,j}$ = actually number of cycles applied to component i at a specific cyclic load level j,
$N_{f\,i,j}(x\%)$ = fatigue life of solder attachment of component i at load level j at $x\%$ failure probability,
β_i = Weibull slope for SM solder attachment of component i.

The differences between CDR, CDR(x%), and $F_\Sigma(N)$ are numerically illustrated in Table 3. From the numbers in Table 3 and additional analysis, it is clear that while CDR and CDR(x%) have some correspondence with $F_\Sigma(N)$, they do not have any physical meaning by themselves. CDR is independent of any failure distribution and CDR(x%) has meaning only when it is unity assuring that the actual and the acceptable failure probabilities are equal. Of course, neither CDR nor CDR(x%) can account for multiple components.

TABLE 3. Numerical Comparison of Reliability Indicators CDR (Eq. 7), CDR(x%) (Eq. 8), and $F_\Sigma(N)$ (Eq. 9).

Weibull Slope,	Acceptable Failure Probability,	Actual Cumulative Failure Probability at N Cycles,	Cumulative Damage Ratio to Failure Probability x,	Cumulative Damage Ratio Based on Mean Life,
β	x	$F_\Sigma(N)$	CDR(x%)	CDR
2	0.01 %	1.0000 %	10.0249	0.1204
2	0.01 %	0.1000 %	3.1630	0.0380
2	0.01 %	0.0100 %	1.0000	0.0120
2	0.01 %	0.0010 %	0.3166	0.0038
2	0.01 %	0.0001 %	0.0982	0.0012
4	0.01 %	1.0000 %	3.1662	0.3470
4	0.01 %	0.1000 %	1.7784	0.1949
4	0.01 %	0.0100 %	1.0000	0.1096
4	0.01 %	0.0010 %	0.5619	0.0616
4	0.01 %	0.0001 %	0.3201	0.0351

It is therefore quite clear, that there is not much point in specifying or determining the CDR's, but that the most effective way to systems reliability is the cumulative failure probability.

DESIGN FOR RELIABILITY

Design for Reliability (DfR) can be accomplished by using the relationships discussed earlier. Given design parameters, such as use environment, design life, and acceptable failure probability, adjusting the parameters that are variable by the designer, such as component size (number of I/O's or pitch), attachment type (leadless or leaded), solder joint height, lead stiffness, coefficient of thermal expansion of the circuit board, can assure product that is reliable in the long term.

Sometimes these choices require compromises or higher costs; but, it certainly is preferable to assure reliability than to have product failures at the customer.

Some of the cyclic environments in Table 2 violate the caveats stated previously. In particular, Cyclic Environments 4 to 7 violate Caveat 2 and Cyclic Environments 22 to 27 violate Caveat 3.

While Cyclic Environments 4 to 7 violate Caveat 2, and this violation has non-conservative consequences, the small number of cycles involved—18 cycles over 20 years of service for Cyclic Environments 4 to 7 combined—results in only very small damage from these environments. Thus, the overall error introduced by using Eq. 1 is very small.

The Cyclic Environments 22 to 27 violate Caveat 3. However, this violation has conservative consequences and these environments occur only for a combined 7 cycles over 20 years of service. Thus, the damage for these environments is very small, and as a consequence the overall error introduced by using Eq. 1 is very small.

SUMMARY

'Design for Reliability' for surface mount solder attachments requires up front design measures that include the physical parameters controlling the damage mechanisms leading to failure, consideration of the statistical failure distribution inherent in failure mechanisms like fatigue, and knowledge of the use conditions for the product.

Representative use conditions for the design however have to frequently reflect the large variation in the actual use conditions experienced in the field over long design lives. This is particularly true for the avionics thermal cyclic environment described in this paper, but would be equally as complex for other applications, such as automotive environments.

The necessary information for a successful 'Design for Reliability' for such complex environments has been presented in this paper.

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Werner Engelmaier has over 28 years of experience in electronic packaging and interconnection technology. Known as "Mr. Reliability" in the industry, he is President of Engelmaier Associates, Inc., a firm providing consulting services on reliability, manufacturing, and processing aspects of electronic packaging and interconnection technology. Prior to forming his own company, Mr. Engelmaier was a Distinguished Member of the Technical Staff at AT&T Bell Laboratories for 24 years.

Mr. Engelmaier is the author of over 100 technical publications in a variety of fields related to electronic packaging and has been awarded a number of patents in these areas. He has conducted many tutorial workshops, and has contributed to numerous task forces, specifications, standards, and design guides. He serves as Chairman of the IPC Product Reliability Committee and is a member of the Editorial Advisory Board of *Electronic Packaging and Production* magazine. He has been the recipient of many honors and awards, including the Distinguished Technical Staff Award from AT&T Bell Laboratories in 1986; the IEPS Electronic Packaging Achievement Award in 1987; and the IPC President's Award in 1988.

Born in Vienna, Austria, Mr. Engelmaier holds Mechanical Engineering degrees from Technologisches Gewerbe-Museum (TGM), Vienna, Austria; the University of South Carolina; and the Massachusetts Institute of Technology.

Address: Engelmaier Associates, Inc.
23 Gunther Street
Mendham, NJ 07945

Prospects of Solder Paste in Ultra Fine Pitch Era*

Dr. Manchao Xiao, Kevin J. Lawless, and Dr. Ning-Cheng Lee
Indium Corporation of America
Utica, NY
Tel: (315) 853-4900 Fax: (315) 853-4320

Abstract

The 12 mil pitch processing is achievable with solder paste. It may also be the limit of solder paste printing technology, mainly due to the scooping problem associated with thin stencils. With decreasing pitch size, both smear and insufficiency rate increase. Tapering of stencil aperture helps thick stencil prints, but hurts on thin stencil printing. Aperture with orientation parallel to squeegee movement results in a higher print defect rate. Overall, use of fine powders is the most effective means to meet most challenges. It helps on achieving high performance in printability, tack, and non-slump, with acceptable trade-off in rheology and tack time. Solder balling may be the primary hurdle. The problem may be resolved by using inert reflow atmosphere or via flux chemistry improvements. A metal load of 90.5 to 91% seems to be the optimum for most properties.

Key Words: Solder Paste, Fine Pitch, Print, Slump, Solder Ball

I. Introduction

In the development of surface mount technology, solder paste has been the most important material in forming solder joints at the assembly of PCB's. Among other features, low cost, high yield, ease of processing, and high joint qualities are the primary merits of using solder paste. However, with the advancement of ultra fine pitch technology, especially at the pitch level below 20 mil, the applicability of solder paste is now being challenged. In this work, the potential of solder paste in the ultra-fine-pitch application is investigated based on the analysis of materials and flux chemistries. Factors considered include printability, paste rheology, wetting, solder balling, tack, tack time, slump, oxide content, etc. Besides the paste, other factors such as the quality of PCB's, components, stencils, printers, and pick-and-place equipments, which are critical to the successful implementation of paste-based process, are also briefly discussed.

II. Experimental Design

1. Solder Paste Materials

In this study, the potential of paste was investigated typically with the use of a RMA flux and 90.5% Sn63 solder powder. The solder powder used varies in mesh size. In the case of -325/+500 mesh, the metal load further varies from 30 to 92%, as shown in Table 1.

Table 1. Composition of Sn63 solder pastes

No.	Powder mesh size	Average powder diameter (micron)	Paste metal load (w/w %)
1	-200/+250	66.0	90.5
2	-200/+325	60.4	90.5
3	-250/+325	53.0	90.5
4	-325/+400	42.0	90.5
5	-325/+500	35.9	30.0
6	-325/+500	35.9	60.0
7	-325/+500	35.9	88.0
8	-325/+500	35.9	89.0
9	-325/+500	35.9	90.0
10	-325/+500	35.9	90.5
11	-325/+500	35.9	91.0
12	-325/+500	35.9	92.0
13	-400/+500	32.0	90.5
14	-400/+635	26.6	90.5
15	-500/+635	23.0	90.5

The solder powder size is determined via sieve analysis, and the average powder diameter is expressed as "number average powder diameter", as defined below:

At first, let V_n be the number average powder volume,

$V_n = V / N$ where V = total volume of powder
N = total number of particles

Then the number average powder diameter D_n can be derived using the relation: $V_n = (4\pi / 3)*(D_n / 2)^3$
Hence,

$$D_n = \{ \Sigma W_i / \Sigma (W_i / D_i^3) \}^{1/3} \quad \text{----------} \quad (1)$$

where W_i is the weight fraction of powder with diameter D_i, and both W_i and D_i can be determined from sieve analysis.

2. Printability

In order to determine the potential of solder paste in ultra-fine-pitch printing process, not only the paste printing performance was evaluated, but also the factors and mechanisms which may affect the print quality were studied. The factors covered in this work include stencil thickness, pitch dimension, aperture orientation, stencil opening tapering-treatment, and solder powder size. In the study of stencil related factors, unless otherwise specified, the pastes used were 90.5% in metal load, with powder diameter varied from 23 to 66 microns. The results of the first print were used to represent the printability for the corresponding test conditions.

Equipment For Printability Study

The stainless steel stencils used were manufactured by IRI using laser cut technology. The test parameters include stencil thickness, pitch dimension design, aperture treatment, and orientation, as shown in Table 2. The printer used was Universal Model 4114A, and was equipped with metal squeegee. The test was conducted with on-contact print onto a polymethyl methacrylate board. The squeegee speed used was 1.0 inch per second.

For the pitch dimension design, each pitch pattern includes small, medium, and large aperture sizes, as listed in Table 3. Unless otherwise specified, the average performance of all three opening sizes is used to represent the print performance at the corresponding pitch.

Table 2. Stencil parameters

Parameter	Test design
Thickness (mil)	2, 3, 4, 5, 6, 7, 8
Pitch (mil)	8, 12, 16, 20, 25, 30, 50
Aperture orientation	Perpendicular or parallel to squeegee movement
Aperture treatment*	Tapered or non-tapered

* With tapering treatment, the bottom side opening is 1 mil (25.4 microns) wider in both width and length than the top side opening.

Table 3. Stencil aperture dimension design

Pitch (mil)	Aperture width (mil)	Spacing (mil)	Aperture length (mil)
8	3	5	40
	4	4	
	5	3	
12	5	7	40
	6	6	
	7	5	
16	7	9	50
	8	8	
	9	7	
20	8	12	50
	10	10	
	12	8	
25	11	14	60
	13	12	
	15	10	
30	13	17	60
	15	15	
	17	13	
50	20	30	80
	25	25	
	30	20	

Print Defect Classification

Empirically, the printability can be defined as being inversely proportional to the print defect level. The print defect was determined by examining the print quality on the board using a 20X to 80X optical microscope. In order to evaluate the printability quantitatively, primary print defect types, smear and insufficiency, are further categorized. The possible impact of each print defect subgroup on the reflowed solder joint quality is then weighed, as shown in Table 4. A weight of one represents a totally unacceptable print defect for each pad or each spacing considered. In general, the smear is weighed by the possibility of forming a solder bridge, and the total smear defect is expressed as percentage of total number of spacing involved. On the other hand, the insufficiency is weighed by the potential of forming an open joint or a badly starved solder joint, and the total insufficiency defect is expressed as percentage of total number of pads printed. The overall printability is accordingly assessed by summing up the defect rate of the two

Table 4. Classification of print defects

Major defect type	Defect subgroup	Weight as defect
Smear	Point smear	0.1
	Point smear to 50% smear	0.3
	> 50% smear	1
Insufficiency	70 to 90% volume deposit	0.3
	< 70% volume deposit	1

types of print defect. For example, a print with a complete insufficiency for all pads but no other defects will have a defect rate of 100%, while a print with a total smear for all spacings plus a complete insufficiency for all pads will have a defect rate of 200%.

Effect of Stencil Thickness

The effect of stencil thickness on defect level and defect type is illustrated in Figure 1. Each data point represents the average of all data for results on stencil with the designated thickness. In general, the overall defect level rapidly increases with increasing stencil thickness. The print defect mainly constitutes of insufficiency, which also increases rapidly with increasing stencil thickness. Apparently this is due to incomplete filling and clogging phenomena. However, at 2 mils stencil thickness, the insufficiency rate is substantially higher than the major trend. The unusually high defect rate associated with 2 mil stencil prints holds true not only for coarse powders, but also for fine powders, as shown in Figure 2. Results indicate that in all incidents, tha print defect rate is always higher than 1%. This is considerably higher

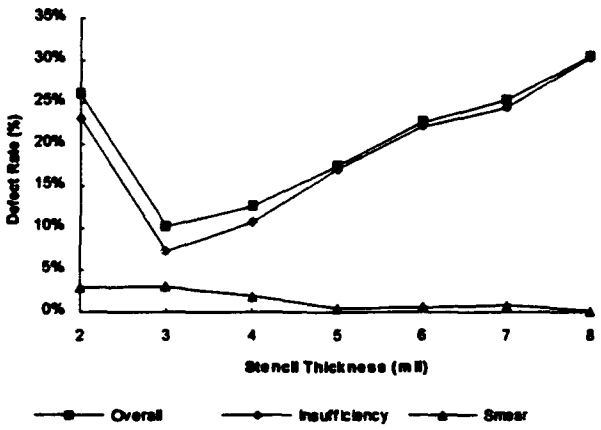

Figure 1. Effect of stencil thickness on print defect

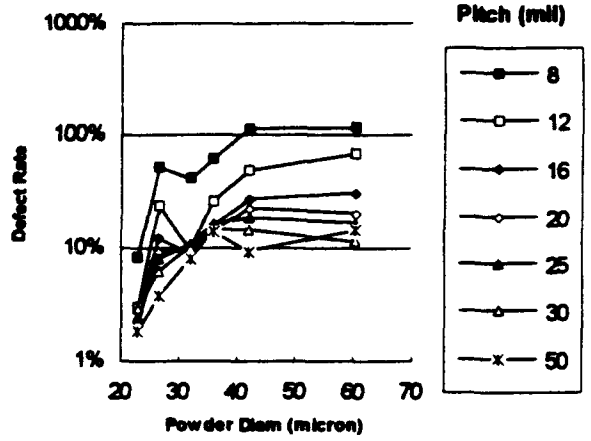

Figure 2. Results of printability test using 2 mil stencil. Both powder size and pitch dimension varied.

than the 0.1% criterion, as will be discussed later. This abnormity is attributed to the scooping effect occurred during printing.

Compared with insufficiency, smear is relatively insignificant and generally decreases with increasing stencil thickness. Presumably the printing pressure exerted onto the paste decreases gradually with increasing distance from the top side of the aperture. As a result, the driving force for the paste to ooze into the space between the stencil and the board also becomes lower when a thicker stencil is used.

Although the defect rate decreases with decreasing stencil thickness, the scooping related upswing of defect rate at 2 mils stencil thickness indicates that the minimum stencil thickness acceptable for solder paste printing is approximately 3 mils. This phenomenon appears to be an inherent limitation of printing process for high viscosity paste materials. Hence this "3 mils" may be the limit of improving the ultra-fine-pitch printability via thinner-stencil approach.

Effect of Tapering Treatment of Stencil Openings

Table 5 compares the defect rate of tapered patterns versus that of non-tapered patterns. The data are the averaged performance of all pastes and all stencils. It is interesting to note that the tapered pattern shows a considerably higher smear rate than non-tapered pattern. Presumably this can be attributed to the wider opening of the bottom side of the tapered aperture, which allows the paste to flow more readily under the printing pressure. In general, the tapering treatment reduces the overall defect rate slightly, primarily due to the reduction of insufficiency rate.

Table 5. Effect of tapering treatment on defect rate

Aperture feature	Smear defect rate	Insufficiency defect rate	Overall defect rate
Non-tapered	0.86%	20.95%	21.81%
Tapered	1.97%	19.19%	21.16%
Tapered / non-tapered	2.29	0.92	0.97

Apparently this can be related to the better release of the tapered shape.

However, as shown in Figure 3, the tapering treatment gradually shows an adverse effect on the overall defect rate with decreasing stencil thickness. This is mainly due to the increasing contribution of smear to the overall defect rate, as demonstrated in Figure 1. For ultra-fine-pitch printing process, since the stencil thickness is expected to become smaller, it is very questionable whether the tapering treatment is still desirable or not.

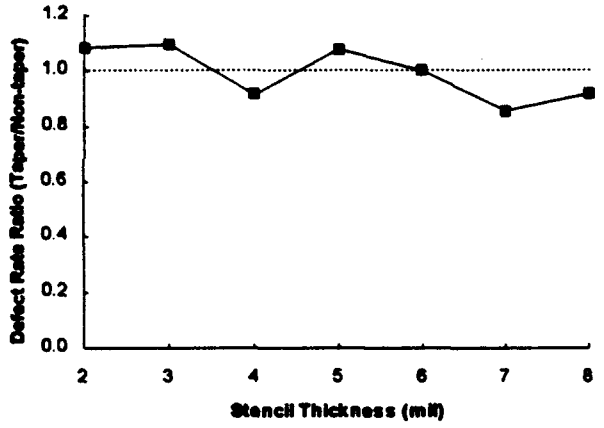

Figure 3. Effect of stencil thickness on defect rate ratio (tapered / non-tapered)

Effect of Pitch Dimension

Apparently the finer the pitch, the poorer the printability, as exemplified in Figure 4. Results shown here are the averaged performance of all pastes with 90.5% metal load using all stencils. The print defect rate increases very rapidly with decreasing pitch at pitch level below 30 mils. As indicated in Figure 5, the primary defect type is insufficiency. This is quite understandable, since more and more clogging is expected to occur with decreasing aperture size. However, it is quite a surprise to learn that the smear increases at an even higher rate with decreasing pitch. In Figure 5, the contribution of smear to the overall

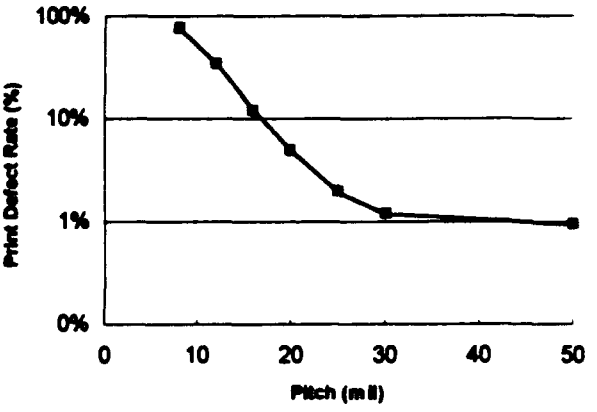

Figure 4. Effect of pitch dimension on defect rate

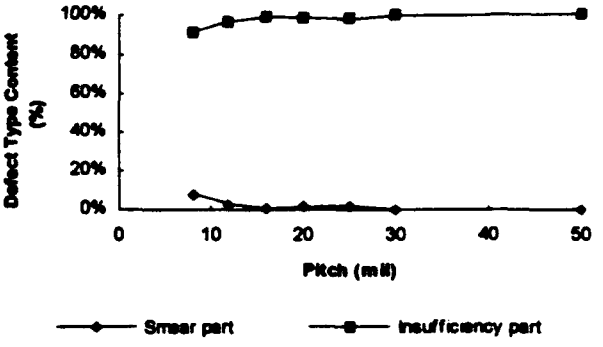

Figure 5. Effect of pitch dimension on distribution of various type of defect

defect increases from virtually 0% to 8% when the pitch decreases from 50 to 8 mils. This probably can be explained by the relative rate of paste oozed out versus spacing reduction. Hypothetically, the amount of paste oozed out should decrease with decreasing aperture size due to decreasing print pressure transmitted to the paste near the bottom side of aperture. On the other hand, spacing reduction would enhance the probability of smear. It is possible that the spacing reduction effect overcompensates the paste leakage reduction effect, resulting in an increasing contribution of smear to the overall defect rate.

Effect of Aperture Orientation

In order to explore the possibility of improving printability through stencil pattern design, the effect of aperture orientation on defect rate is examined, with data shown in Figure 6. In this study, the aperture longitudinal axis is either parallel or perpendicular to

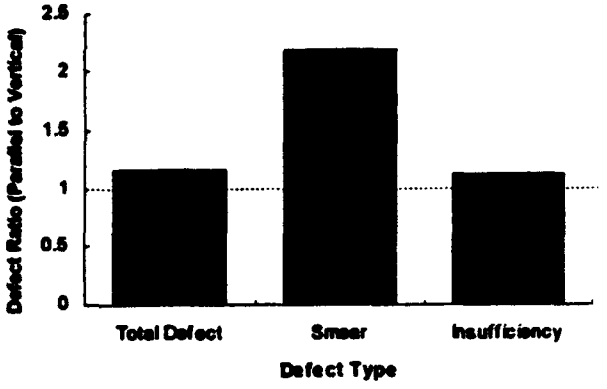

Figure 6. Effect of aperture orientation on defect rate

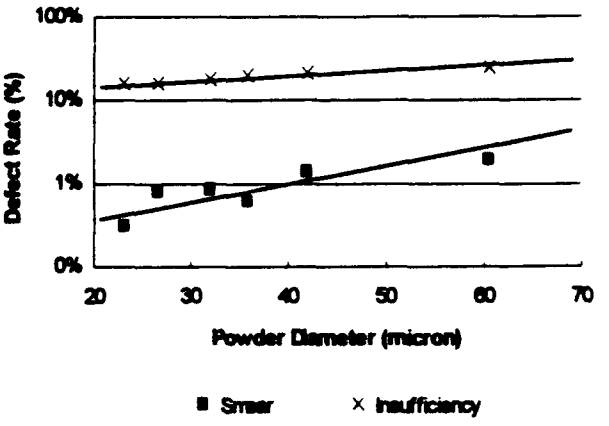

Figure 7. Effect of powder size on defect rate

the squeegee movement. Each data point corresponds to the averaged performance of all pastes with 90.5% metal load tested on all stencils. The results indicate that the parallel orientation shows a higher defect rate than that of perpendicular orientation. The adverse effect of parallel orientation is particularly pronounced for smear type defect.

This can be explained by the gasketing effect and restrained flow effect. In the case of perpendicular orientation, the aperture axis is parallel to the squeegee axis. Hence the whole aperture is virtually pressed simultaneously by the squeegee during printing. This will not only create a very tight gasketing effect, but also leave no free opening for the paste to flow out of the aperture. The former effect will result in a lower smear rate, while the latter will ensure a better filling of aperture with paste, and consequently a lower insufficiency rate.

The definite effect of aperture orientation on defect rate suggests that the printability probably can be improved through redesigning the pattern orientation. Presumably this can be accomplished relatively easily through modifying the alignment of the printed circuit board on the printer.

Effect of Powder Size

To address the printability issue of ultra-fine-pitch, use of fine powder is probably the most frequently adopted approach. Figure 7 shows the effect of solder powder size on defect type and defect rate. Data represent the averaged performance of pastes with 90.5% metal load tested on all stencils. Both smear and insufficiency are reduced with decreasing particle size. The relation observed for insufficiency appears to be self-evident, since the chance of clogging should be reduced with decreasing powder size, especially for very small apertures. However, it is not quite obvious why smear is also reduced with decreasing powder size. Presumably this can be accounted for by the restrained paste flow due to the higher viscosity and higher tack associated with finer powder, which will be discussed later.

Acceptable-Printability Criteria

Table 6 displays the typical aperture width and stencil thickness used in the industry for 20 to 50 mils pitch pattern. In general, the stencil thickness is approximately one half or slightly less than one half of the aperture width, which in turn is about one half of the pitch value. The "standard stencil thickness" column shows the most commonly used thicknesses. Using this relationship, the standard stencil dimensions for 8 to 16 mil pitch can be accordingly derived through extrapolation, and are shown in parenthesis in the same table.

Realistically, whether a solder paste can be used for printing certain fine pitch pattern in SMT processing should be judged by the print performance using a reasonable stencil thickness, or "standard stencil thickness". Therefore, although the print defect of each pitch design are evaluated thoroughly from 2

Table 6. Relation between pitch and stencil dimensions

Pitch (mil)	Typical aperture width (mil)	Typical stencil thickness (mil)	Standard stencil thickness (mil)
50	25-30	8-12	8
30	15-18	7-9	7
25	12-15	6-7	6
20	10-13	5-6	5
16	(8-10)		(4)
12	(6-7)		(3)
8	(4-5)		(2)

to 8 mils stencil thickness in this work, the acceptability of a certain paste in printing for a certain pitch level, or acceptable-printability, is assessed according to the printability at the corresponding "standard stencil thickness".

In addition, a maximum print defect rate of 0.1% is used for determining whether a solder paste is acceptable or not for SMT process. Hence the acceptable-printability for certain pitch pattern can be defined as a print performance with no more than 0.1% defect rate when tested at the "standard stencil thickness".

Prospects of Solder Paste in Printability

By accepting the criteria defined above for acceptable-printability, the maximum powder size allowed for each pitch level can be accordingly determined, with the results shown in Figure 8. For 8 mil pitch, none of the pastes tested is qualified as being acceptable. On the other hand, for 50 mil pitch, all pastes are acceptable and show a defect rate considerably lower than 0.1%.

The relation in Figure 8 can be expressed by the following equation:

$$D = 0.059 + 0.066\,W \quad \text{---------- (2)}$$

where D = maximum powder diameter (mil) allowed
W = pitch dimension (mil)

Table 7 displays the predicted maximum powder size allowed, according to equation (2). Also shown is the typical aperture width for each pitch level. In general, the maximum powder size allowed is approximately 1/7 of the typical aperture width. For 16 and 12 mil pitch patterns, the maximum powder size allowed is roughly equivalent to -400/+635 and -500/+635 mesh, respectively. Although powders of both mesh ranges are finer than the currently prevailing -325/+500 mesh powder used for fine pitch application, mass production of those finer powders are believed to be still feasible. However, this "1/7" relation may hold true down to 12 mil pitch only. For 8 mil pitch, the "standard stencil thickness" is expected to be 2 mil. Although the desirable ultra-fine powder might still be manufacturable, the scooping mechanism discussed above virtually eliminates the possibility of achieving a good print. Improvement in printability via optimization of other parameters, such as aperture orientation, is expected to be fairly minute, if any at all. Perhaps the hurdle for 8 mil pitch printability can be overcome through the use of a thicker stencil plus a powder even finer than 14.9 microns in diameter. Yet this possible solution is intensely challenged by the solderability requirement, as will be discussed later.

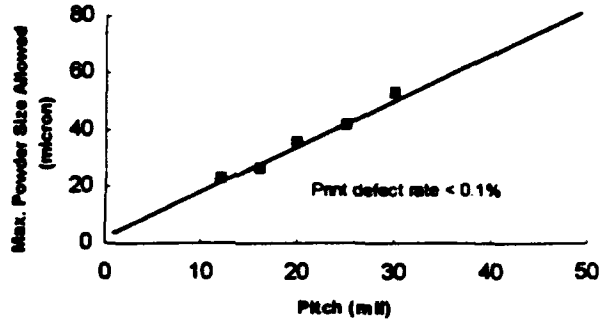

Figure 8. Relation between pitch dimension and maximum powder size allowed

Table 7. Predicted maximum powder size allowed for SMT process

Pitch (mil)	Typical aperture width (mil)	Predicted maximum powder diameter allowed (mil)	(micron)
50	25	3.37	85.5
30	15	2.04	51.9
25	13	1.71	43.5
20	10	1.38	35.1
16	8	1.12	28.4
12	6	0.85	21.7
8	4	0.59	14.9

Overall, it can be summarized that it should be possible to print solder paste successfully down to 12 mil pitch. Beyond that, a major breakthrough may be needed in either printing technology or paste materials.

3. Paste Rheology

The printability behavior in general is a result of the paste rheology, and the data discussed above are based on the use of a fixed flux/vehicle rheology. To explore the potential of solder paste in printing, the possibility of improving the printability through regulating the paste rheology should not be ignored. The two most important parameters of paste rheology are viscosity and thixotropic property. Powder size, metal load, and flux/vehicle rheology are the major elements commonly used to regulate the paste rheology. In this work, the flux/vehicle itself is kept constant, and the effect of powder size and metal load on paste rheology are investigated. The viscosity is determined with a spiral pump viscometer at 25°C.

The shear rate varies from 3, 5, 10, 20, to 40 rpm. For viscosity comparison, the reading at 10 rpm is used.

Effect of Metal Load

At first, the effect of metal load on rheology is studied. Generally speaking, the solder paste can be regarded as a composite system. Since the volume content of filler, or solder powder, appears to be more meaningful for structure-property correlation study of a composite system, all the relations will be based on the volume content parameter. Figure 9 shows the relation between metal weight content and metal volume content for the Sn63-containing solder pastes used in this study. The volume content of solder first increases slowly, then rises rapidly with increasing solder weight content. The rapid rise of volume content results in an even more rapid rise in viscosity of paste, as shown in Figure 10.

Theoretically, the maximum powder volume content is 74% for a monodispersed sphere system with face centered cubic packing structure, or 68% for a body centered cubic packing structure. Solder powder, although exhibits a broader size distribution, displays a considerably lower packing density. The tap density of Sn63 solder powders typically is about 4.9 gm/cm^3, and is not sensitive to the powder size distribution. This tap density is equivalent to 59% solder volume occupancy. For solder paste used here, a 59% solder volume content is equivalent to 92.5% metal content. In other words, 92.5% (w/w) is the maximum metal load allowed for pastes. Therefore, this rapid increase in viscosity for solder content beyond 50%(v/v), or 89.5%(w/w), most likely can be attributed to the onset of formation of powder clusters. As a result, the viscosity of a high metal load paste starts being dictated by the solder powder continuity, and variation in the flux/vehicle viscosity will have a relatively minor effect on the paste viscosity.

The thixotropic property can be expressed by the thixotropic index (TI), which is defined as the negative value of the slope of the linear regression line for log viscosity vs log (shear rate) relationship, as shown in equation (3). The higher the TI value, the more thixotropic the material is.

$$Y = a + b*X \quad \text{----------} \quad (3)$$

where Y = log value of viscosity
a = material constant
b = slope of the linear regression line for X and Y relation, equals (-TI)
X = log value of shear rate of viscometer

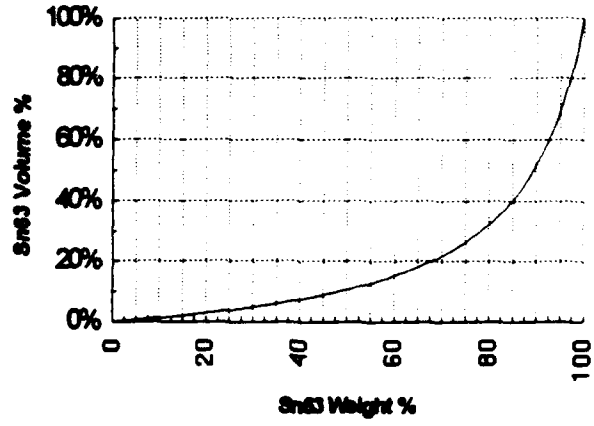

Figure 9. Relation between metal volume % and metal weight % of Sn63 solder paste (sp.gr. : Sn63 8.40, flux/vehicle 1.00)

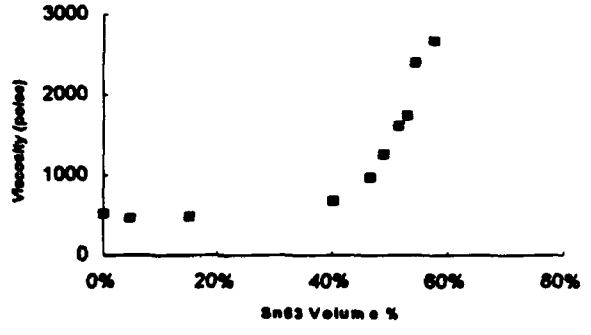

Figure 10. Relation between viscosity and metal volume content of Sn63 solder paste

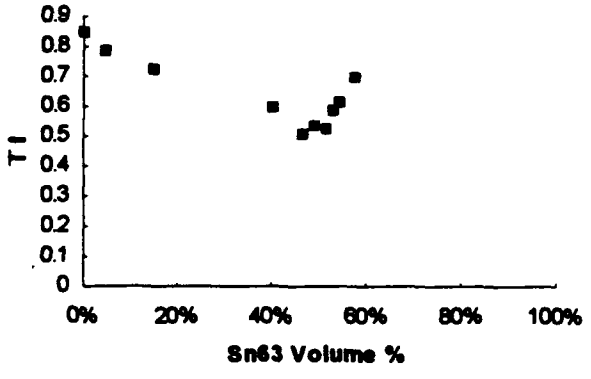

Figure 11. Relation between metal volume content and TI of Sn63 solder paste

Figure 11 shows the effect of solder volume content on TI. It is interesting to note that the TI decreases first, then increases with increasing solder volume content. The turning point occurs at around

50% solder volume. The initial decrease in TI can be attributed to the dilution effect of the thixotropic flux/vehicle by the powder. The upswing of TI with increasing metal content can be attributed to the pseudo-thixotropic-additive effect of the powder cluster network. It indicates that the TI value can be regulated through metal content adjustment for further improvement in printability.

Effect of Powder Size

The size of solder powder also plays a significant role in paste rheology. Figure 12 shows that the viscosity increases with decreasing powder size. This can be explained by the increasing particle surface area associated with finer powder. This results in an increasing interaction force between flux and powder, and consequently a higher viscosity. In the case of thixotropic property, the finer powder results in a lower TI value, as indicated by Figure 13. Again, this can be attributed to the greater interaction force between flux and the finer particles. This interaction force, being primarily a surface adsorption phenomenon, is believed to be non-thixotropic in nature. Since it contributes to the paste viscosity, the material is accordingly expected to be less thixotropic. Hence, the finer powder needed for ultra-fine-pitch printing will increase the paste viscosity and decrease the thixotropic property. Assuming that the "Harada Operating Window" is also applicable to ultra-fine-pitch printing, both influences would demand more from the flux/vehicle rheology development to compensate for the changes caused by using finer powders.

Overall, paste rheology can be further optimized by varying the metal load and flux rheology for better printability in an ultra-fine-pitch application. The fine powder size required for good printability, on the contrary, places some burden on the rheology improvement effort.

4. Slump

Slump is the major cause of solder bridging at reflow. In addition, it also contributes to solder balling. Depending on the paste formulation, it may even occur at room temperature. However, most often it occurs during reflow. Whether the slump can be eliminated or controlled is very critical for successful implementation of ultra-fine-pitch processing.

Test Method

The slump test is conducted using an 8 mil thick stencil, with a pattern similar to that of IPC-A-21

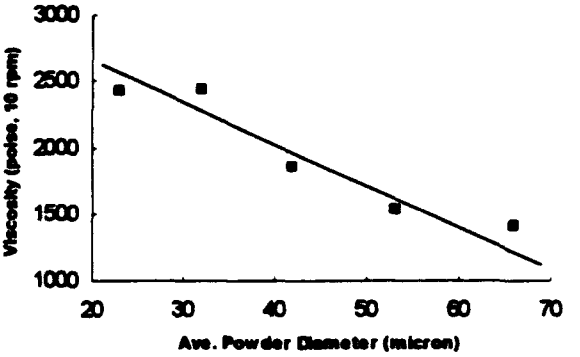

Figure 12. Relation between poowder size and viscosity of Sn63 solder paste

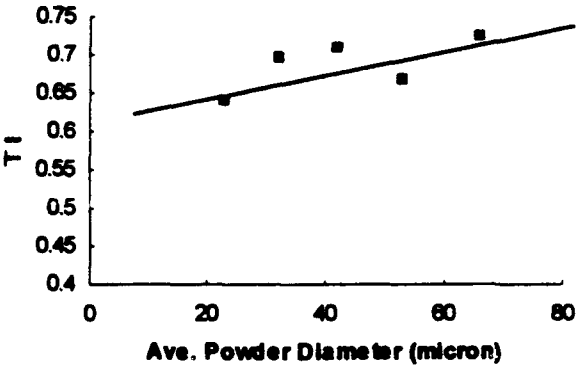

Figure 13. Relation between powder size and TI of Sn63 solder pastes with 90.5% metal content

Table 8. Slump test pattern design

Large aperture (25*80 mils)		Small aperture (13*80 mils)	
Spacing (mil)	Spacing/ aperture width	Spacing (mil)	Spacing/ aperture width
13	0.52	6	0.46
16	0.64	8	0.62
19	0.76	10	0.77
22	0.88	12	0.92
25	1.00	14	1.08
28	1.12	16	1.23
31	1.24	18	1.38

design [1]. The dimension of this pattern is specified in Table 8. There are two horizontal and two vertical test sites for each spacing specified. The slump performance at 25°C (cold slump) and 100°C (hot slump) is determined after the printed sample has been conditioned for 10 minutes and 1 hour, respectively, at the designated temperature. Also

shown in Table 8 is the ratio of spacing to aperture width. The slump is expressed as Slump Index (SI), which is evaluated by first identifying the largest spacing bridged by paste for both small aperture and large aperture patterns. The average of those ratios for the corresponding largest bridged spacing is then calculated and is used to represent the slump performance. In other words, the slump is measured by the value of the largest normalized spacing bridged. A value of 1.31 represents all spacings bridged, while an extrapolated value of 0.31 represents no bridging observed at all.

The slump evaluation method described above assumes that the slump of small aperture pattern is comparable to the slump of large aperture pattern when both are expressed in SI values, and therefore one single averaged SI value is sufficient to reflect the slump potential despite the variation in pitch dimension. In general, this assumption is found to be valid in this study.

Effect of Metal Load

Figure 14 shows the relation between metal load (w/w) and slump. All pastes used in this study have a powder size of -325/+500 mesh. At 25°C, no bridging occurred at all. At 100°C, there is no bridging observed for 91 and 92% metal load. However, at metal load below 90%, the hot slump increases rapidly with decreasing metal load, and reaches 1.1 for 88% metal load. The low slump of the high metal load paste can be attributed to the high viscosity, as implied by Figure 10. For fine pitch pattern design, the spacing to pad width ratio normally is around 1 or slightly less than 1. This suggests that a metal load of 90.5% or higher should satisfy the non-bridging need of ultra-fine-pitch application.

Effect of Particle Size and Particle Size Distribution

The paste samples used in this work are 90.5% in metal load. According to Figure 12, reducing the powder size will increase the paste viscosity, hence is expected to result in a reduction in the slump. This is found to be true, as shown in Figure 15 for cold slump and in Figure 16 for hot slump. Also shown in these two figures is the effect of particle size distribution on slump. Generally speaking, a wide powder size distribution aggravates the slump when compared with narrow size distribution. However, in all cases, the SI is found to be no more than 0.6, which is considerably lower than the spacing to pad width ratio used by the industry.

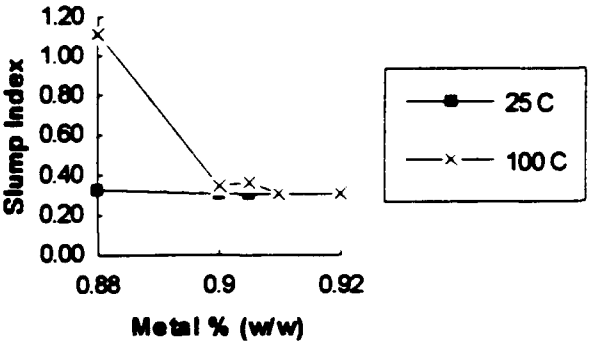

Figure 14. Relation between metal load and slump for Sn63 solder pastes with -325/+500 mesh powder

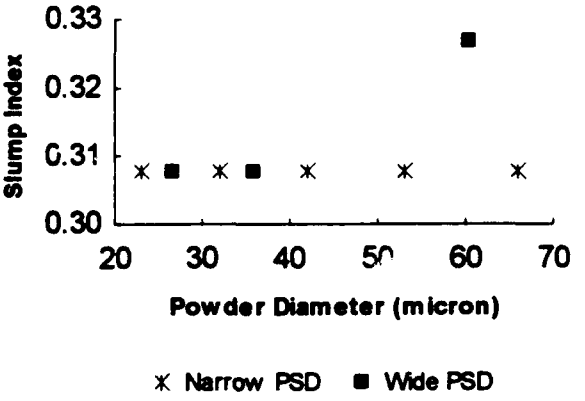

Figure 15. Effect of powder size and PSD on cold slump for 90.5% Sn63 solder paste

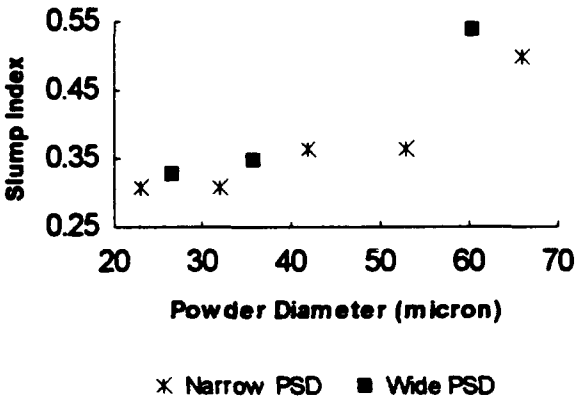

Figure 16. Effect of powder size and PSD on hot slump for 90.5% Sn63 solder paste

Therefore, there is practically no slump concern for all powder sizes at metal load of about 90.5% or higher. In addition, the non-slump performance can be further enhanced through the use of finer powder or a narrower particle size distribution.

5. Tack and Tack Time

Since the trend of SMT is shifting towards finer dimension, it becomes a concern whether the tack and tack time can meet the challenge in the ultra-fine-pitch era. Here the "tack" is defined as the tackiness reading determined on a freshly printed paste, and the "tack time" is the time elapsed for the paste to reach its maximum tackiness value when the printed sample is exposed to the ambient environment. In this work, the impact of particle size, metal content, and print dimensions on both properties are investigated. Unless otherwise specified, the test method of ANSI/IPC-SP-819 is used for determining both tack and tack time.

Effect of Powder Size

As indicated in Figure 17, the tack increases with decreasing powder size. This eases the concern for the tack in ultra-fine-pitch era. The tack is believed to be proportional to the adhesive and cohesive force of the paste. The adhesive force is governed by the flux/vehicle alone. However, the cohesive force increases with decreasing powder size due to the increase in the powder surface area of the paste, and consequently results in an increase in the tack.

Figure 18 shows a typical behavior of tackiness versus time for the paste, with a maximum tackiness observed at 5 days. The effect of particle size on tack time is displayed in Figure 19. Although the data scattering is quite significant, it can be seen that the tack time increases first, then reaches the peak at approximately 35 microns powder diameter, then decreases with decreasing powder size. The initial increase can be explained by the increasing diffusion path length for the solvent to reach the paste surface before it dries out. In addition, the increase in powder surface area also helps to retain the solvent longer due to increasing powder-solvent surface adsorption. The declining trend beyond the peak can probably be attributed to the skin formation effect caused by excessive chemical reaction between flux and the fine powder. This dry skin formed consequently would reduce the adhesive force of the paste, and result in a short tack time.

Overall, reducing the powder size results in a significant increase in the tack, but only a moderate variation in the tack time.

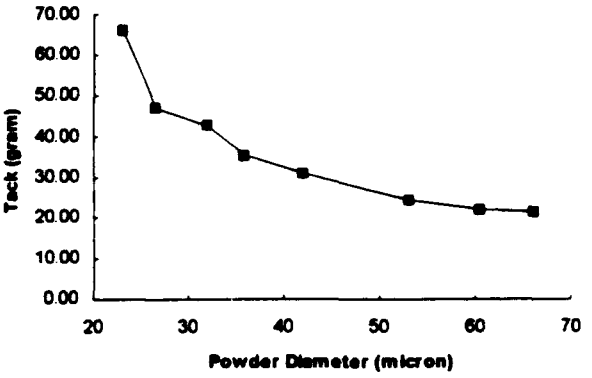

Figure 17. Relation between powder size and tack for Sn63 solder pastes with 90.5% metal load

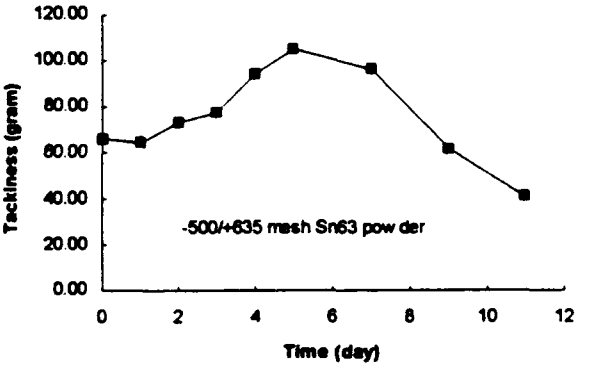

Figure 18. Relation between tackiness and exposure time for paste with 90.5% Sn63 (-500/+635 mesh)

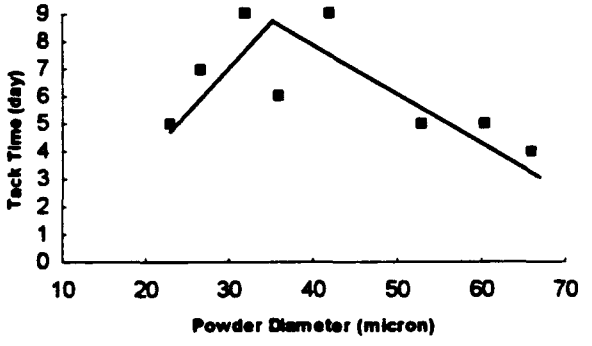

Figure 19. Effect of powder size on tack time of Sn63 solder pastes with 90.5% metal content

Effect of Metal Load

The relation between metal content and tack is fairly complicated, as shown in Figure 20. With increasing metal load, the tack drops rapidly at first, then declines slowly until 40% volume content. This

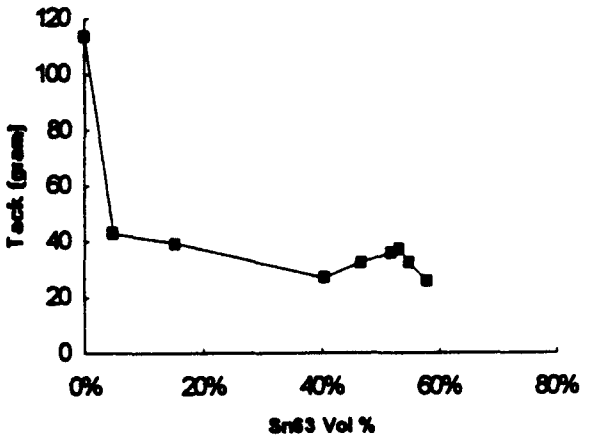

Figure 20. Relation between tack and metal content of Sn63 solder paste (-325/+500 mesh powder)

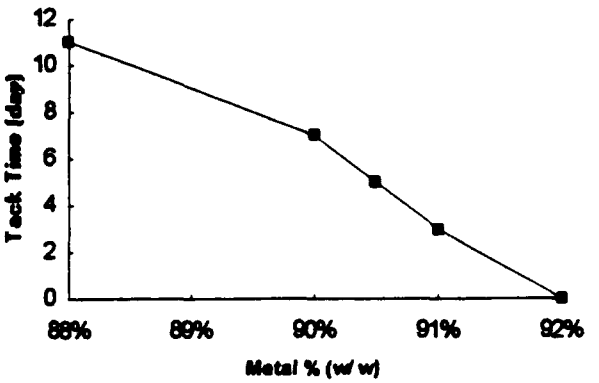

Figure 21. Relation between metal load and tack time of Sn63 solder paste with -325/+500 mesh powder

declining trend most likely can be related to the sample thickness at test. In general, the lower the powder content, the more the paste can be squashed during the tack test, and consequently the smaller the clearance between the test probe and substrate will be. Since a smaller clearance favors a better gasketing effect upon detachment, a higher tack is then expected. At metal loads beyond 40%, the tack shows an increase followed by a decrease with further increase in the metal load. The increase in tack can be attributed to the increasing cohesive force due to increasing filler reinforcement effect. The decrease in the tack at metal volume content beyond 53% presumably can be related to the gradually increasing insufficiency of the flux/vehicle binder for the powders. Overall, all cases show a tack value reasonably high for metal content up to 58% (v/v), suggesting that tack is not a critical issue for ultra-fine-pitch application. The local tack maximum observed indicates that 53% (v/v), or 90.5% (w/w), may be the optimum metal content for achieving a high tack value.

Figure 21 displays the relation between metal load and tack time. Data indicate that virtually there is no tack time observed at 92% metal load, and the tack time increases with decreasing metal load. Apparently the increasing tack time associated with increasing flux content can be easily attributed to the increase in solvent content. Also, a metal content of no more than 91% (w/w) seems to be desirable for achieving a reasonable tack time.

Effect of Print Dimensions

Probably the miniaturization of print dimensions will be the factor concerned most when attempting to achieve an acceptable tack and tack time for ultra-fine-pitch process. To examine the impact of print dimensions, the tack and tack time are directly determined on samples with various pitch dimensions. The stencil used is 6 mils in thickness, with the pattern dimensions specified in Table 9. The paste used is 90.5% Sn63, with -500/+635 mesh in powder size.

Table 9. Stencil pattern design for print dimensions factor study

Pitch (mil)	Stencil design		
	Aperture length (mil)	Aperture width (mil)	No. of pads under tack test probe
50	75	24	4
25	100	13	7.5
20	45	13	9

Figure 22 shows the relation between tackiness and time elapsed. Since the paste quantity covered by the tack test probe varies with varying pitch dimension, the tackiness measured is expressed in gram force per unit area printed with paste. In addition, the load on the probe is also adjusted so that 15.3 g/(mm^2 paste) pressure is applied onto the paste in each case. The results indicates that the tack is about 2 gram/(mm^2 paste), despite of the variation in pitch dimension. However, the tack time does vary somewhat with varying pitch size. Data shown in Figure 23 demonstrate that the tack time decreases moderately with increasing exposure area of paste. In this case, the surface area between the neighboring pads is not considered as valid exposure due to locally hindered ventilation, hence is not included in the surface area calculated.

Therefore, it appears that, although the tack value itself is not affected, the tack time does shorten

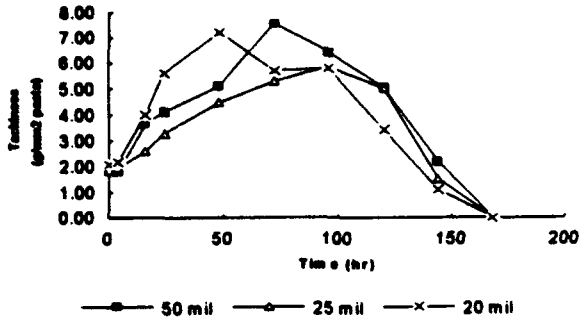

Figure 22. Relation between tackiness and exposure time for various pitch dimensions

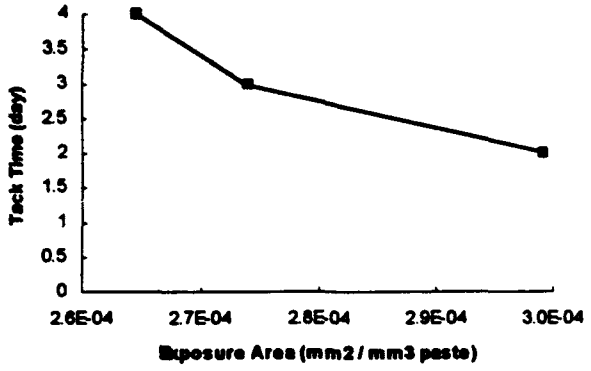

Figure 23. Relation between tack time and exposure area per unit volume of paste

somewhat with reducing pitch dimension and accordingly demand a better in-line process-timing-control for ultra-fine-pitch application. The moderate decline of tack time with decreasing pitch dimension suggests that the tack time is not a limiting factor on using solder paste.

6. Solder Balling

Presence of solder balls could promote the possibility of circuit short. This is particularly true for no-clean application. To investigate the potential for solder balling, pastes with variation in metal content and powder size were tested. The test method used was ANSI/IPC-SP-819. In each case, six specimens are tested, and all of the solder balls generated are counted or estimated. The total number of the solder balls is used to represent the solder balling performance.

Figure 24 shows the effect of metal load on the number of solder balls. The powder used in this study is -325/+500 mesh size. The results indicate that the number of solder balls first decreases rapidly, then

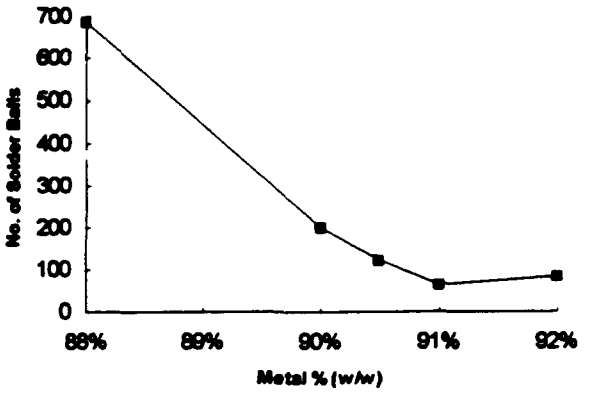

Figure 24. Effect of metal content on solder balling behavior of Sn63 solder pastes with -325/+500 mesh powder

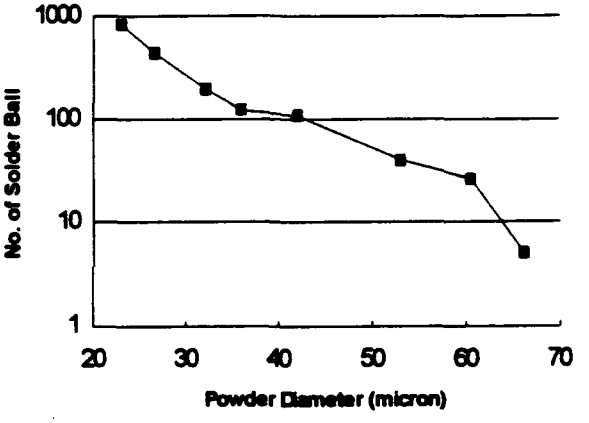

Figure 25. Effect of powder size on solder balling behavior of Sn63 solder pastes with 90.5% metal load

reaches the minimum value at 91% (w/w), followed by a slight increase with increasing metal content. The initial drop in the number of solder balls with increasing metal load is mainly due to the decreasing slump. The slight upswing of solder balling at metal content beyond 91% is attributed to the increasing insufficiency of relative flux capacity. Here the flux capacity is defined as the molar concentration of effective flux functional groups in the flux/vehicle.

The effect of particle size on solder balling is shown in Figure 25. With decreasing particle size, the number of solder balls increases drastically. Presumably, the more powder grains involved in coalescence process, the more chance of having some particles left behind. This probability-based hypothesis is verified by plotting the number of solde balls against the number of particles per unit mass of

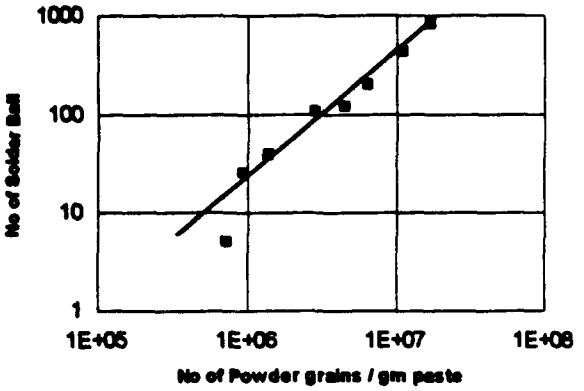

Figure 26. Relation between powder concentration and solder balling behavior of Sn63 solder pastes with 90.5% metal load

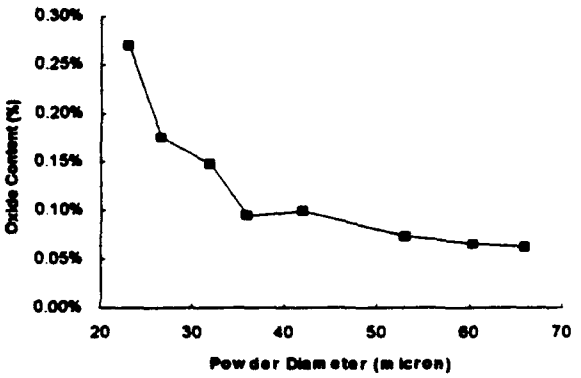

Figure 27. Relation between Sn63 powder size and oxide content

paste, as shown in Figure 26. Here both parameters are expressed in log scale, and a linear relationship is observed. Besides the probability mechanism, the high solder oxide content of fine powders may also be responsible for the high solder balls frequency, as will be discussed in the next section.

Overall, it can be summarized that, to achieve a solder-ball-free performance in ultra-fine-pitch application, the optimum metal load is around 91% (w/w). Furthermore, a significant improvement in flux chemistry, particularly in the area of flux capacity, is needed in order to use fine powders for no-clean air reflow process.

Solder Oxide

It seems to be reasonable to assume that the solder oxide layer thickness is the same regardless of the powder size. Thus, theoretically, decrease in powder size will result in an increase in powder surface area, and proportionally a higher oxide content. This is found to be true, as shown in Figure 27. The high oxide content associated with the fine powders is believed to be also responsible for the poor solder ball performance discussed above. In this test, the oxide content is assessed by determining the weight difference of the powders before and after coalescence caused by fluxing reaction. Hence the oxide content here refers to the total weight percentage of tin oxides and lead oxides in the Sn63 solder powders.

However, further analysis indicates that the constant oxide thickness assumption stated above holds true only to a certain extent. Figure 28 shows that the oxide content per unit surface area of the powder grains, or the oxide thickness, remains constant with decreasing particle size until 35 microns

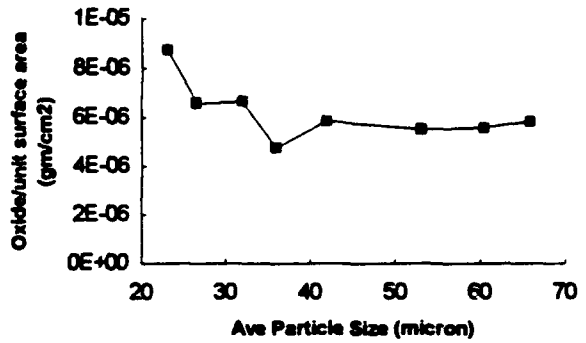

Figure 28. Relation between Sn63 powder size and oxide thickness

powder diameter. Further decrease in powder diameter results in an increase in the oxide thickness. This unexpected results suggest that the oxide content is not only a function of powder surface area, but possibly also a function of powder manufacturing method. Perhaps the thicker oxide layer exhibited by the very fine powders is caused by the excessive sieving processes during powder classification stage.

Since a fine powder is required for ultra-fine-pitch application, and since the oxide content increases sharply with decreasing powder size, it becomes essential to explore the limit of flux capacity in handling solder oxide. If the amount of solder oxide demands a flux capacity more than a reasonable paste composition can afford, it will be impossible to utilize such a powder. Per the worst case scenario, all oxides are assumed to be SnO_2. Accordingly, the fluxing reaction required to eliminate the oxide can be represented as below.

$$SnO_2 + 4\,RCO_2H \rightarrow Sn(RCO_2)_4 + 2\,H_2O$$

The minimum amount of flux needed can be calculated accordingly for any given molecular weight of RCO_2H molecule. In the case of a 90% (w/w) metal load solder paste, the maximum amount of flux allowed is 10% of paste. By expressing the minimum amount of flux needed in terms of fraction of the maximum flux quantity allowed, the possibility of having a high capacity flux can be thus estimated for any given solder oxide content. The smaller the fraction is, the greater the possibility will be. Figure 29 shows the potential of having a high capacity flux for pastes with various powder sizes. The hypothetical molecular weights used here are 100, 200, 400, and 800, respectively. In all cases, the fraction calculated is considerably less than 1. This suggests that there is a great potential for the paste technology to improve further in performances, such as solder balling, when using fine powders.

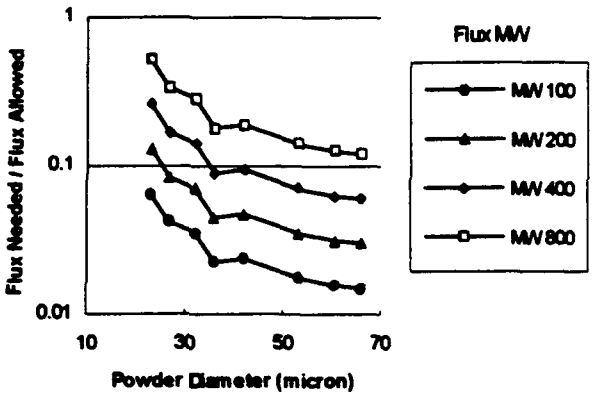

Figure 29. Relation between Sn63 powder size and the potential of having a high capacity flux for a solder paste with 90% metal load

7. Wetting

Hypothetically, when the particle size is getting finer, the flux consumed by the solder oxide will increase, and consequently there will be less amount of flux available for removing the substrate metallization oxide. Since a fine powder is needed for ultra-fine-pitch printing process, the wetting capability of the paste should be accordingly ensured. In this study, the wetting test is conducted on the oxidized copper coupon. Each copper coupon is first precleaned in a 10% HBF_4 aqueous solution, followed by baking on a 230°C hot plate surface in air for 1, 3, 9, and 27 minutes, respectively. The paste is then printed onto the coupons with a stencil used in the slump test. All samples prepared are then reflowed through a typical reflow profile in air in an in-line infrared furnace. The wetting behavior for each paste and each oxidized coupon is then examined under a 10X optical microscope. In order to quantitatively evaluate the wetting capability, a numbering system is established, as defined in Table 10. Therefore, depending on the extent of spreading, a number is then assigned to each test specimen. The wetting capability of each paste is then expressed by the Wetting Index (WI), which is the sum of the numbers assigned to the specimens using coupons oxidized for 1, 3, 9, and 27 minutes, respectively.

Table 10. Definition of numbering system for wetting characterization

No	Class	Description
0	Poor	Solder beads up
1	Fair	Solder wets partial deposited area
2	Good	Solder fully wets deposited area
3	Excellent	Solder wets beyond deposited area

Figure 30 shows the effect of powder size on wetting. All pastes used here exhibit a metal content of 90.5% (w/w). Surprisingly, the powder size seems to have no effect at all on the wetting characteristics of pastes. Presumably, the elimination of solder oxide may be a relatively simple task for the flux, and the wetting characteristics is mainly dictated by the substrate metallization.

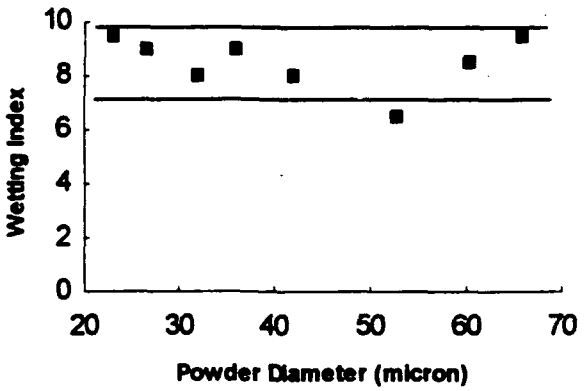

Figure 30. Effect of Sn63 powder size on wetting for solder paste with 90.5% metal load

The effect of metal content on wetting is studied with pastes using -325/+500 mesh powders, and the results are shown in Figure 31. The WI first decreases slowly with increasing metal load, then drops rapidly at metal load beyond 91%. Since the solder oxide has a negligible effect on wetting, the relation observed here probably can be, at least partially, attributed to the slump factor.

Therefore, as long as the metal content can be kept below 91% (w/w), the wetting capability of

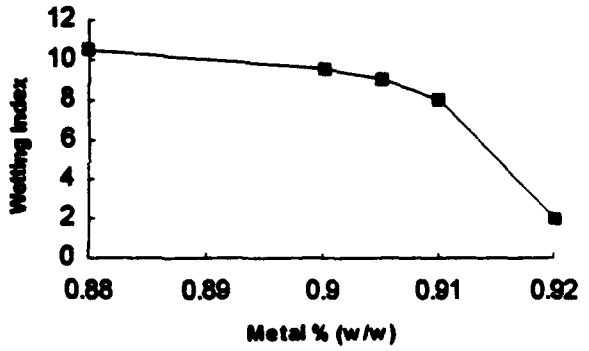

Figure 31. Effect of metal load on wetting for solder paste with -325/+500 mesh powder

solder paste essentially is not an issue for ultra-fine-pitch application.

III. Discussion

1. Print test

In this work, the print defect evaluation is based on the results of the first print. Compared with the results of subsequent prints, in general, this choice yields a higher insufficiency rate but a lower smear rate. However, despite the difference in the relative weight of defect type, the major trends observed in this study should still hold true.

The printability results are obtained from the laser cut stencils which have not been electropolished. Probably a coarser powder can be used to achieve a high print quality if the aperture smoothness can be improved. This will help the soldering performance, hence enhance the potential of paste for ultra-fine-pitch use.

2. Paste Rheology

All pastes used in this study are based on the use of a single flux/vehicle for the sake of consistency and simplicity. Therefore, the potential of parameters such as powder size and metal load is not fully explored. In addition, the printing parameters are kept constant also. It is reasonable to expect that the parameters listed above can be further optimized, and the prospects of solder paste should be even more promising than what observed in this work.

3. Reflow Atmosphere

Typically, the use of an inert reflow atmosphere will result in a much better performance in solder balling and wetting. This will allow the use of some fine powders which performed poorly under air-reflow condition. In other words, the limit of solder paste application can be pushed in a finer pitch direction.

4. Printed Circuit Boards

For printed circuit boards, the condition of pads is the most crucial factor. Boards with poor solderability will not only result in a weak bonding, but also aggravate the voiding problem. In the past, HAL solder coating used to be the prevailing approach to retain the solderability. However, with the reduction in pitch dimension, the effectiveness of this tinning method becomes questionable. Too thick a tinning will result in a dome shaped solder bump, which in turn will cause poor prints. When the tinning is too thin, the copper-tin intermetallics will degrade the solderability of the pads very rapidly. Recently the organic protective coating and Au plating have received more and more attention. Both approaches appear to be very promising on retaining the solderability of pads without much trade-off.

Regardless of which surface protection method to be used, the solderability of the pads needs to be improved further. This is mainly due to the reduction in solder paste thickness deposited, hence also a reduction in the flux quantity available for removing the pad oxide.

5. Components

Coplanarity is probably the most important parameter associated with components which affects the solder paste processing yield. Current unofficial industry standard is 0.004". Apparently this can not satisfy the need of ultra-fine-pitch process. It has been reported [2] that the coplanarity tolerances will eventually be halved to 0.002" due to improvements in lead conditioning process. However, even at this new horizon, the need for 12 mil pitch process, where the paste thickness is probably 3 mils, can only be barely satisfied. It is the authors' opinion that the coplanarity needs to be held down to 1 to 1.5 mils to meet the requirement of 12 mil pitch.

6. Printers

For fine pitch printing process, the registration is a critical factor to a successful printing. A precision of 0.001" is considered adequate for 12 mil application. Due to the increasing incidents of smear defect with decreasing pitch dimension, as discussed above, an automatic stencil bottom wiping design is

recommended. A hard squeegee with durometer reading no less than 90 becomes necessary for a good print definition. The emergence of metal squeegee provides an satisfactory alternate in this regard. Printing speed is also another important parameter. As a rule of thumb, the finer the pitch, the slower the squeegee speed. This is primarily due to the increasing restraint on paste flow imposed by the shrinking aperture.

7. Pick-and-Place Equipments

Currently the major improvements seen for components placement are speed and alignment. Chipshooters typically can achieve a speed of 0.14 to 0.29 sec. per component. The alignment of components usually is ensured via the use of vision systems and computer-controlled component-to-component pad alignment [3]. However, the placement force control is still the relatively weak link in this process. Excessive placement force will promote bridging between pads and solder beading [4] around leadless chip capacitors and resistors. Particularly the latter will be a concern for no-clean process.

8. Reliability

With decreasing pitch, the reliability gradually becomes a concern. This is mainly due to the possibility of forming circuit short through entrapment of solder balls and development of electromigration between pads. The former can be improved through the use of an inert reflow atmosphere. Prevention of corrosion-related circuit short, however, demands a combined effort of use of a better and cleaner board material, cleaner components, and a milder flux. In addition, applying a conformal coating onto the assembled boards is expected to enhance the reliability as well.

IV. Summary

The test results of solder pastes for ultra-fine-pitch process can be summarized in Table 11.

V. Conclusions

The 12 mil pitch process is achievable with solder paste. It may also be the limit of solder paste printing technology. Overall, use of fine powders is the most effective means to meet most challenges. It helps achieving high performance in printability, tack, and non-slump, with acceptable trade-off in rheology and tack time. Solder balling may be the primary hurdle. The problem may be resolved by using inert reflow atmosphere. A metal load of 90.5 to 91% seems to be the optimum for most properties.

Table 11. Summary of solder paste potential study

Property	Findings
Printability	1. Thinner stencil print better 2. Minimum 3 mils thickness needed 3. Tapering help thick stencil print, hurt thin stencil 4. Both smear and insufficiency worsen with decreasing pitch dimension 5. Perpendicular better than parallel 6. Finer powder reduce both defect types 7. Powder/aperture ≤1/7 needed for good print 8.12 mils pitch may be print limit
Rheology	1. Metal content can regulate TI and viscosity 2. Fine powder hurt rheology
Slump	1. ≥ 90.5% metal load, fine powder, narrow powder size distribution help achieving low slump
Tack	1. Fine powder help tack 2. 90.5% metal load optimum for tack 3. Print dimension no effect
Tack time	1. 35 μ optimum powder size 2. Metal load ≤ 91% desired 3. Finer pitch hurt tack time slightly
Solder balling	1. Finer powder aggravate problem, due to probability and/or oxide 2. 91% metal load optimum
Solder oxide	1. Oxide layer is thicker for very fine powders 2. Great potential on overcoming oxide of very fine powders via flux
Wetting	1. Powder size no effect 2. 91% metal load optimum

VI. Acknowledgement

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VII. References

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Dr. Ning-Cheng Lee is Manager of Research and Development at Indium Corporation of America, Clinton, New York. He has had experience in polymers and epoxy encapsulants, including 10 years of experience in fluxes and solder pastes development.

Dr. Lee has a Ph.D. in Polymer Science from the University of Akron and a B.S. degree in Chemistry from National Taiwan University. He is a member of ISHM, ACS, and ASM.

Address: Indium Corporation of America
36 Robinson Road
Clinton, NY 13323

CERTIFICATION AND TRAINING TRENDS FOR INDUSTRY AND MILITARY

BY
Mel Parrish
MTTC, COMARCO Inc

ABSTRACT

New challenges of global markets require new workers. Our workers of the future must be knowledgeable, infinitely flexible to new technologies, as well as qualified on existing manufacturing practices. In addition, new technologies must be developed by our laboratory and research organization to meet the industry challenges that are:

Expansion toward global markets

Increased foreign competition

Environmental challenges:
- Elimination of Ozone depleting chemicals / substance (ODC)
- Reduction in the use of volatile organic compounds (VOC)
- Elimination of hazardous alloys in solder (lead)

Diversification of defense industries toward commercial markets while maintaining defense capabilities.

Management philosophy changes, such as "Concurrent Engineering."

Training as well as certification resulting from training becomes the key to all these issues. As the technology changes, qualification of our work force must change as well.

TRAIN OR NOT TO TRAIN

In times of tight budgets, often training is first to feel the pinch. Often this can be a grave mistake. By limiting our work force capability we often adversely affect:

- Production rates
- Processing costs
- Quality
  - Rework
  - Recall (product)
  - Reduced reliability
  - Limited capability for bids

All of these topics relate directly to profit and often survival of our companies.

Training requires correct investment strategies balancing consideration for corporate costs while providing a capable qualified staff and work force. To accomplish this worthy objective, concentration is necessary in those areas that are most productive. Often these are conceptual training topics such as quality concepts that benefit the entire work force as well as management.

Conceptual changes in management philosophy structures toward concurrent engineering or similarity programs is destined to failure if not communicated effectively to workers at all levels. Training is again the key to communicating the concept and persuading the acceptance by employees without misconception of the intended results.

An alternative concept is to hire someone else's qualified and well trained employees and hope for the best.

CERTIFICATION

Certification equates to documentation of the ability in this case of an employee to reach a certain measurable skills when compared to a consistent standard.

Certification requires sponsorship of an organized authority to administer and establish credibility for the program. Any program of certification must provide adequate flexibility to develop concepts of the company and attain standards as well. Defense standards have allowed and encouraged this flexibility since the advent of DOD-STD-2000 and MIL-STD-2000 in 1987 to current. A certification program that is inflexible discourages innovative and progressive approaches to manufacturing.

Certification provides certain advantages to the company:

It insures consistent qualification of employees to minimum standards.

Certification ties the employee to the company that has invested the time and money to effect training and certification as a result of training. If an employee leaves the company, certification should be revoked until the new company accomplishes the necessary certification elements. This guarantees return on investment through maintenance of capability, and the option discussed previously "Hire someone else's trained employee" is no longer a valid consideration.

Certification provides assurance of adequate performance and confidence for the customer in contract awards. It establishes creditability for the prospective awardee to meet or exceed necessary provisions of contract.

It establishes a communication link for technology progression between contractors to the aid of all industry. We sorely need to get correct information to the field and those who need it most. The vast majority of companies do not (and should not) invest large sums of scarce capital to provide research development and laboratory facilities to evaluate products and processes that could be more effectively passed on to through certification channels.

Certification provides an organization to distribute information when questions arise in the manufacturing environment. Much of our current work day is spent providing advise on technical questions posed by graduates or potential graduates of our current certification program. The information interchange is a positive step in maintaining consistency as well as providing a conduit of information concerning lessons learned to those that require this information. This prevents companies from making the same mistakes again and again at great cost that must be eventually passed on to the customer.

Certification builds employee confidence and participation as a member of the organization. It provides the challenge of a quantitative goal for personal and company improvement.

CERTIFICATION TRENDS

Defense standards are currently relaxing the stringent certification requirements of past standards. Individual service standards of the 1980's were very explicit concerning certification issues to the point of approval for company internal training plans. With the evolution of common defense standards this requirement was removed and was yet further liberalized in revision A to MIL-STD-2000, except as modified by specific contract provisions.

Commercial standards such as IPC-A-610 and J-STD 001 are being developed to include certification requirements as a result of training. This concept fits well into the ISO 9000 series standards which enforce consistent qualification of staff with a structured training program. Many companies have pursued MIL-STD-2000 certification for this reason alone. They have no contract with defense procurement however anticipate ISO 9000 registration as being necessary to pursue contracts with European customers.

European concepts related to manufacturing traditionally include certification of employees to disciplines such as electronic manufacturing. Our new ties in global markets as well as the need for competitiveness forces us to look again at our own standards such as J-STD-001 if it is to be accepted as an international standard. To be attractive to European organizations and companies certification will probably be necessary here as well.

TRAINING METHODS

Many exciting new (or so termed new) concepts are available to industry that are departures from traditional techniques. Certainly today no one that can read has been able to avoid the computers. They have become a way of life and training is no exception. In fact the computer is one of the most powerful tools we have to employ. Computer aided instruction (CAI), Multimedia presentations and many of the other concepts have increased exponentially with the advent of readily accessible bulk storage techniques. The concept is by no means new but certainly is improved. Many early attempts (1970's) were total disasters where no training objectives were met other than learning how to operate the computer training system. Certainly we learn from past lessons and todays product is vastly improved over those early attempts. The cost of development of this type of system is quite large and may not be justified for individual small companies. However, it may be justified when a larger audience can be considered. We are currently working with a graphic development company to create just such a product for general soldering concepts. Often times this type of training tool can effectually augment training being accomplished by other methods such as laboratory demonstrations be conducted by an instructor or hands on operation of machine processes.

Small companies may find that dedicated resources for training are not cost effective. In these cases, third party training may prove the most effective approach. Under this concept a training company with enough demand of resource investment is contracted to conduct training for a company rather dedicating funding sources that are utilized for infrequent periods. This concept allows for a high level of qualification of the instructor or other training elements such as computer based training that would not be possible for smaller companies.

The common standby is a stand up instructor to teach and coach students through the learning process. In this case quality of objective achievement is dependent to a great deal on the skills of the instructor conducting the training. It is not as consistent as programmed or automated instruction. Lets face it we all have good and bad days which makes us human.

On the positive side, it allows for immediate feedback through interaction, implementation of proper questioning techniques, and audience evaluation. It allows interaction between students as guided by the instructor. Certainly some of the most valuable learning situations we have are the lessons learned as shared between students representing all elements of industry. It is probably the only viable approach when physical skills are the objective or are associated as supporting the end objective through application.

Correspondent or training text is very limited in scope and application. It relies on the students ability to comprehend concepts with no other interaction or support. It can in some cases be fairly effective when applied to an audience that is intended to progress from a consistent level of understanding and its limitations are fully understood by the developer.

Trial and error unfortunately is another technique that is far to often applied to our industry. Errors can be extremely costly in time and money. "Here is a new IR convection oven. Set it up and start production on the 42 module next month." The negative consequences of this approach far outweigh the positive.

The best approach is often one that employs combinations of several of these techniques, using the best of each for the advantage of the training opportunity.

DEFENSE ISSUES

As stated previously, revision A to MIL-STD-2000 relaxed some provisions of the defense certification program. It still requires trained and certified operators but does not specifically require any tie to certification authority and as such breaks the tie to consistency and standardization from one company to another. A great deal of carry over in expertise is provided by previous defense certification programs but in many cases has left small or new companies without the background and information to conduct their operations in a manner that prevents contractual issues that equate negatively to product reliability and performance.

In todays world political environment the need for new weapons systems is being reduced, and as a result upgrade, retrofit, or modification of existing systems is becoming necessary. This introduces a new challenge for standardization functions of defense procurement. Often these upgrades are competitively bid by internal defense organizations. The lack of consistent rework/repair and retrofit technique to accomplish these tasks provides a playing field that is not quite level. An initiative to standardize practices, processes and techniques will be necessary for future projects and consistent qualification of operators should be provisioned.

COMMERCIAL ISSUES

Commercial IPC standards have established the process to conduct certification which ties the authority to which training will be conducted and contracts will be issued. The concept appears to be fully supported by the membership organization. This is, to say the least, interesting given the progression of defense standards in the opposite direction especially considering the competitive nature of the commercial industry element.

Industry sorely needs the common manufacturing standard that was envisioned in early attempts with defense standards. Working to one set of rules, while somewhat limiting in initiative and creativity, allows consistency in understanding and compliance with requirements. Leveling the playing field is a noble venture worth the effort.

CONCLUSION

Training is a major critical element that will determine our success in future markets when considering the issues now facing our industry.

We have to learn to work smarter and to work be smarter we need effective training on techniques that are evolving daily in our industry.

Certification provides organization and consistency as well as credibility of our technical training programs just as applied to our schools of higher academics.

Mel Parrish is Manager of the Manufacturing Technology Training Center (MTTC) based in Ridgecrest, California. He is the principal investigator of the MTTC for developing and marketing curriculum for advanced research under a cooperative agreement with the Naval Air Warfare Center Weapons Division (NAWCWPNS), China Lake, California.

Mr. Parrish has been fully involved in technical training and training management for over 16 years. He has supported the operations of the former Electronic Technology Training Center and the Soldering Technology Branch under NAWCWPNS operations for 7 years. He is involved in the Navy Electronic Assembly Technology Working Group and IPC committees for IPC-A-610 (Workmanship and Acceptability of Electronic Assemblies) and J-STD-001 (Requirements for Electrical and Electronic Assemblies).

Address: MTTC, Comarco Inc.
P. O. Box 1420
543 Graaf Street
Ridgecrest, CA 93556